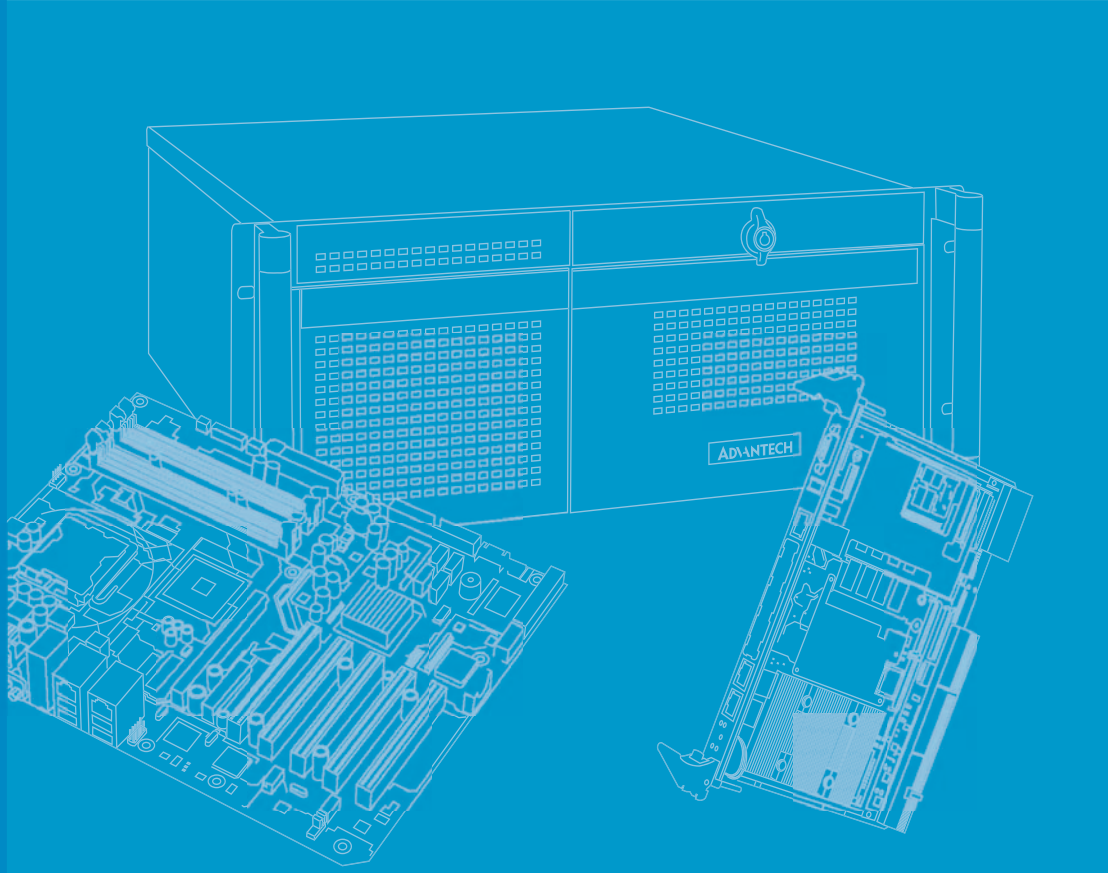

User Manual

MIC-3396

6U CompactPCI 4th Generation Intel® Core™ i3/i5/i7 Processor Blade with ECC support

ADVANTECH

Enabling an Intelligent Planet

Copyright

Acknowledgements

All other product names or trademarks are properties of their respective owners.

Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are classified into different classes, divisions and groups, based on hazard considerations. This equipment is compliant with the specifications of Class I, Division 2, Groups A, B, C and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions, which if not observed, can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data. e.g.:*

There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Note! *Notes provide optional additional information.*

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such, in writing, to: support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item is not accord with the table, please contact your dealer immediately.

- MIC-3396 all-in-one single board computer (CPU heatsink and PCH heatsink included) x1
- Daughter board for SATA HDD x1(Assembled)
- HDD tray and screws package x 1
- Solder-side cover (Assembled) x1
- RJ45 to DB9 cable x1
- Warranty certificate document x1
- Safety Warnings: CE, FCC class A

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

We Appreciate Your Input

Please let us know of any aspect of this product, including the manual, which could use improvement or correction. We appreciate your valuable input in helping make our products better.

Contents

Chapter 1

Hardware Configuration

This chapter describes how to configure MIC-3396 hardware

1.1 Introduction

The MIC-3396 is a high performance, power efficient CompactPCI single-board computer based on the Intel® Core™ i3/i5/i7 microprocessors. The MIC-3396 delivers breakthrough energy-efficient performance for CompactPCI platforms. The Intel® Core™i3/i5/i7 provides enhanced energy-efficient performance to help equipment manufacturers optimally balance processing capabilities within power and space constraints. The advanced smart cache of Core™ i3/i5/i7 dynamically allocates the shared L2 cache across cores and optimizes use of memory subsystem bandwidth to accelerate out-of-order execution. A prediction mechanism reduces the time in-flight instructions have to wait for data. The new pre-fetch algorithms move data from system memory into fast L2 cache in advance of execution.

The Core™ i3/i5/i7 combines the benefits of two high- performance execution cores with intelligent power management features to deliver significantly greater performance per watt over previous Intel processors. The two execution cores share a high-performance, power-optimized 5GT/s DMI bus to access the same system memory. To save power, address and data buffers are turned off when there is no activity.

The MIC-3396 maximizes I/O throughput with PCI Express (PCIe) technology. An on-board 8 GB of 1600 MHz DDR3L memory is provided with a combination of SO-DIMM up to max. 8 GB of 1600 MHz DDR3L as option. It supports a fast Serial-ATA interface to an on-board hard drive.

1.2 Specifications

1.2.1 CompactPCI Bus Interface

The MIC-3396 is compliant with PICMG 2.0 Rev. 3.0. It supports a 64-bit / 66 MHz or 33MHz PCI bus for up to 7 CompactPCI slots at 3.3 V or 5 V VIO. The MIC-3396 is hot-swap compliant (PICMG 2.1) and conforms to the CompactPCI Packet Switching Backplane specification (PICMG 2.16) as well as the CompactPCI System Management Specification (PICMG 2.9).

The board can be configured as a system master or a drone board. In drone mode it only draws power from the CompactPCI backplane and is not active on the CompactPCI bus. However, PICMG 2.16 is still fully supported in this mode.

1.2.2 CPU

The MIC-3396 supports Intel® 4th generation Core™ i3/i5/i7 Haswell processor family with clock frequencies up to 2.7 GHz and a Direct Media Interface (DMI) up to 5GT/s.

Intel® 4th generation Core™ i3/i5/i7 processors are validated with Intel® mobile QM87 chipset. This chipset provides greater flexibility by deploying the latest virtualization, multi-threading and I/OAT acceleration techniques, as well as remote asset management capabilities, and improved storage speed and reliability.

Supported processors are listed in the table below. The Intel® 4th generation Core™ i3/i5/i7 processors support up to two cores / four threads at 2.7 GHz / 2.4 GHz and 3 MB / 6MB cache.

1.2.3 Processor

Table 1.1: Processor Type									
Intel CPU Model Number	**CPU architec-ture**	**# Cores**	**# Threads**	**Freq.**	**Cache**	**DMI**	**CPU TDP**	**Package**	**Required airflow**
i3-4100E	Haswell (22nm)	2	4	2.4 GHz	3MB	5GT/s	37W	FCBGA	30 CFM
I5-4402E	Haswell (22nm)	2	4	1.6 GHz	3MB	5GT/s	25W	FCBGA	30 CFM
I5-4400E	Haswell (22nm)	2	4	2.7GHz	3MB	5GT/s	37W	FCBGA	30 CFM
I7-4700EQ	Haswell (22nm)	4	8	2.2GHz	6MB	5GT/s	47W	FCBGA	30 CFM

Note! *Because power consumption and thermal restrictions vary between different CompactPCI systems, please double check these items before installing a higher speed CPU not listed in the table above.*

1.2.4 BIOS

An 8 MB SPI flash contain a board-specific BIOS (from AMI) designed to meet industrial and embedded system requirements.

1.2.5 Chipset

The Intel Mobile QM87 chipset provides excellent flexibility for developers of embedded applications by offering improved graphics and increased I/O bandwidth over previous Intel chipsets, as well as remote asset management capabilities and improved storage speed and reliability.

The Mobile Intel QM87 chipset offers up to 5 GT/s for fast access to peripheral devices.

It delivers outstanding system performance through high bandwidth interfaces such as PCI Express, Serial ATA and Hi-Speed USB 2.0 and USB 3.0.

1.2.6 Memory

The MIC-3396 has up to 8 GB of onboard with ECC support DDR3L memory. It also has one 240-pin SO-DIMM socket that can accommodate an additional 2GB (max. to 8GB) of memory. The following table shows a list of SO-DIMM modules that have been tested on the MIC-3396.

Table 1.2: Memory Type						
Brand	**Size**	**Speed**	**Vendor PN**	**ECC**	**Pin Count**	**Memory Chip**
ATP	8 GB	DDR3L 1600	AW24P7228BLK0S	Yes	204 - pin	Samsung
	8 GB	DDR3L 1600	XW1628E8GSP9-AV	Yes	204 - pin	Samsung
Transcend	4 GB	DDR3L 1600	A63873-0011	Yes	204 - pin	Samsung

Table 1.2: Memory Type						
Advantech	8 GB	DDR3L 1600	AQD-SD3L8GE16-SG	Yes	204 - pin	Samsung
	8 GB	DDR3L 1600	AQD-SD3L8GE16-MG	Yes	204 - pin	Samsung

Note! *4GB on board memory is optional. Please inform your local sales.*

1.2.7 Ethernet

The MIC-3396 uses one Intel I210-AT and one Intel I217-LM LAN chips to provide 10/100/1000Base-T Ethernet connectivity (LAN1 & LAN2) and three Intel I210-AT LAN chips to provide 10/100/1000Base-T Ethernet connectivity (LAN3~LAN5) via rear I/O, one 10/100/1000Base-T Ethernet can be switched from LAN2 to rear I/O (LAN6). Optional settings for the source of each individual Gigabit Ethernet port can be selected in the BIOS menu. These are mutually exclusive and can be any one of:

- Front I/O (RJ-45)
- Rear I/O (Rear Transition Module)
- PICMG 2.16

1.2.8 Storage Interface

The MIC-3396 supports six SATA III interfaces. One SATA III interface is routed to an onboard 2.5" SATA hard disk drive; one is routed to support an on-board flash (optional); one is CFast connector; two are routed to the rear I/O module via the J3 connector. Currently, Advantech's compatible RIO modules support the SATA II and SATA III devices.

The following table shows a list of SATA HDD and SSD that have been tested on the MIC-3396

Brand	Size	Speed	Vendor PN	Type
WD	120GB	Gen III	WD1200BEVS - 00UST0	HDD
Intel SSD 520 Series	240GB	Gen III	SSDSC2CW240A3	SSD
Plextor	32G	Gen III	PX-32G5Le-72	SSD
Plextor	1TB	Gen III	PX-1TG7Se-72	SSD

1.2.9 Serial ports

One RJ-45 COM1 port (RS-232 interface) is provided on the front panel. Two COM ports are routed to a rear I/O module via the J5 connector.

1.2.10 USB Port

Two USB 3.0 and one USB 2.0 compliant ports with fuse protection are provided. All ports are routed to front panel connectors on the MIC-3396. One USB 3.0 and four USB 2.0 are routed to the rear I/O module via the J3 and J5 connector.

1.2.11 LEDs

Four LEDs are provided on the front panel as follows:

- One blue LED indicates hot swap activity. The blue color indicates that the board may be safely removed from the system

- One yellow color LED indicates HDD activity.
- One green color LED provides power status. When the LED is green, it means power is provided to the board.
- One green color LED indicates “Master” or “Drone” mode. The green color stands for “Master: mode. When the LED is off, the board is in “Drone” mode.
- One green color LED indicates BMC status. When the LED is green, it means BMC is active.

1.2.12 Watchdog Timer

An onboard watchdog timer provides system reset capabilities via software control.

The programmable time interval is from 1 to 255 seconds.

1.2.13 Optional Rear I/O Modules

The RIO-3316 is the optional RTM (also known as rear I/O module) for the MIC-3396. It offers a wide variety of I/O features, such as two or four RJ45 LAN ports, two COM ports, two DVI ports, one USB3.0, one USB2.0 port, one P/S2 port. RIO-3316-D1E can carrier an on-board 2.5” HDD, which support SATA Gen II, and provide two GbE LAN ports, one PS/2, two USB2.0 and one display port. Rear I/O modules are available with following different I/O options:

Table 1.3: RIO-3316 Configuration

RTM Model Number	Rear Panel							On-board Header/Socket/Connector				
	LAN	COM	DVI-I	DVI-D	PS/2	USB 2.0	USB 3.0	Mini-SAS	USB	SATA	SAS / SATA interface	Conn.
RIO-3316-C1E	4	1	1	1	1	1	1	-	2	2	-	J3,J4,J5
RIO-3316-D1E	2	-	-	-	1	2	-	-	2	2	-	J3,J4,J5

1.2.14 Mechanical and Environmental Specifications

- **Operating temperature:** 0 ~ 55 °C (-32 ~ 122 °F)

Note! *The operating temperature range of the MIC-3396 depends on the installed processor and the airflow through the chassis.*

- **Storage Temperature:** -40 ~ 85 °C (-40 ~ 185 °F)
- **Humidity:** 95% @ 40 °C (non-condensing)
- **Humidity (Non-operating):** 95% @ 60 °C (non-condensing)
- **Vibration:** 5~100Hz, 2Grms (without on-board 2.5” SATA HDD)
- **Shock:** 10G (without on-board 2.5” SATA HDD)
- **Bump:** 25G, 6ms
- **Altitude:** 15000ft above sea level at 55 °C
- **Board size:** 233.35 x 160 mm (6U size), 1-slot (4 TE) wide
- **Weight:** 0.8 kg (1.76 lb.)

1.2.15 Compact Mechanical Design

The MIC-3396 has a specially designed CPU heatsink to enable fanless operation. However, forced air cooling in the chassis is needed for operational stability and reliability.

1.2.16 CompactPCI Bridge

The MIC-3396 uses a Pericom PI7C9X130D universal bridge as a gateway to an intelligent subsystem. When configured as a system controller, the bridge acts as a standard transparent PCI Express to PCI/PCI-X Bridge. As a peripheral controller it allows the local MIC-3396 processor to configure and control the onboard local subsystem independently from the CompactPCI bus host processor. The MIC-3396 local PCI subsystem is presented to the CompactPCI bus host as a single CompactPCI device. When the MIC-3396 is in drone mode, the Pericom PI7C9X130D is electrically isolated from the CompactPCI bus. The MIC-3396 receives power from the backplane, and supports rear I/O. The Pericom PI7C9X130D PCI Bridge offers the following features:

- PCI Interface
  - Full compliance with the PCI Local Bus Specification, Revision 3.0
  - Supports 3.3V PCI signaling with 5V I/O tolerance
- Supports transparent mode operations.
- Supports forward bridging
- 64-bit, 66MHz asynchronous operation
- Provides two-level arbitration support for 7 PCI Bus masters
- 16-bit address decode for VGA
- Usable in CompactPCI system slot

Please consult the Pericom PI7C9X130D data book for details.

1.2.17 I/O Connectivity

For MIC-3396, the front panel I/O is provided by two RJ-45 Gigabit Ethernet ports, one RJ-45 COM port, two USB 3.0 and one USB 2.0 ports, one VGA connector, and one XMC/PMC knockout.

Its onboard I/O consists of one SATA channel can be connected to a daughter board for 2.5" SATA HDD and a CFast slot. An on-board NAND flash is as option. Rear I/O connectivity is available via the following CompactPCI connectors:

- **J3:** uses UHM connector, which can support USB3.0, SATA Gen III and PCI Express x8. Two Gigabit Ethernet links to the backplane for PICMG 2.16 packet switch, two SATA Gen III ports, one PCIex8 and two USB 3.0 ports on the RTM.
- **J4:** one LVDS, Audio output, MIC input and one DVI.
- **J5:** One Gigabit Ethernet LAN port, one GbE can be switched from front panel, two COM ports, four USB 2.0, one PS/2 for keyboard/mouse and one DVI port.

1.2.18 PMC (PCI Mezzanine Card) IEEE1386.1 Compliant

Additional I/O or co-processing functionality is supported by add-on PMC modules. The MIC-3396 supports one PMC site that is fully compliant with the IEEE1386.1 PCI Mezzanine Card specification. PMC supports both 64bit / 66 MHz and 32-bit / 33 MHz PCI bus interface and both 3.3 V and 5 V VIO depending on usage.

The two-layer front panel design complies with IEEE 1101.10. Connectors are firmly screwed to the front panel, and a shielding gasket is attached to the panel edge. This reduces emissions and increases protection from external interference.

1.2.19 Hardware Monitor

The SuperIO used by MIC-3396 includes the function of Hardware Monitor, which monitors the critical hardware parameters for the system level. The Hardware Monitor, NCT7904, is attached to the BMC to monitor CPU temperature and core voltage information, when BMC is available.

1.2.20 Super I/O

The MIC-3396 Super I/O device provides the following legacy PC devices:

- Serial port COM1 and COM2 are connected to the rear I/O module or front panel via multiplexer in the FPGA.
- The PS2 (keyboard/mouse) is routed to the rear I/O module.

1.2.21 RTC and Battery

The RTC module keeps the date and time. On the MIC-3396 model the RTC circuitry is connected to battery sources (CR2032M1S8-LF, 3V, 210mAH).

1.2.22 IPMI

The MIC-3396 uses the Intelligent Platform Management Interface (IPMI) to monitor the health of an entire system. An LPC1768 microcontroller provides BMC functionality to interface between system management software and platform hardware. The MIC-3396 implements fully-compliant IPMI 2.0 functionality and conforms to the PICMG 2.9 R1.0 specification. The IPMI firmware is based on proven technology from Advantech. Full IPMI details are covered in Chapter 3.

1.3 Functional Block Diagram

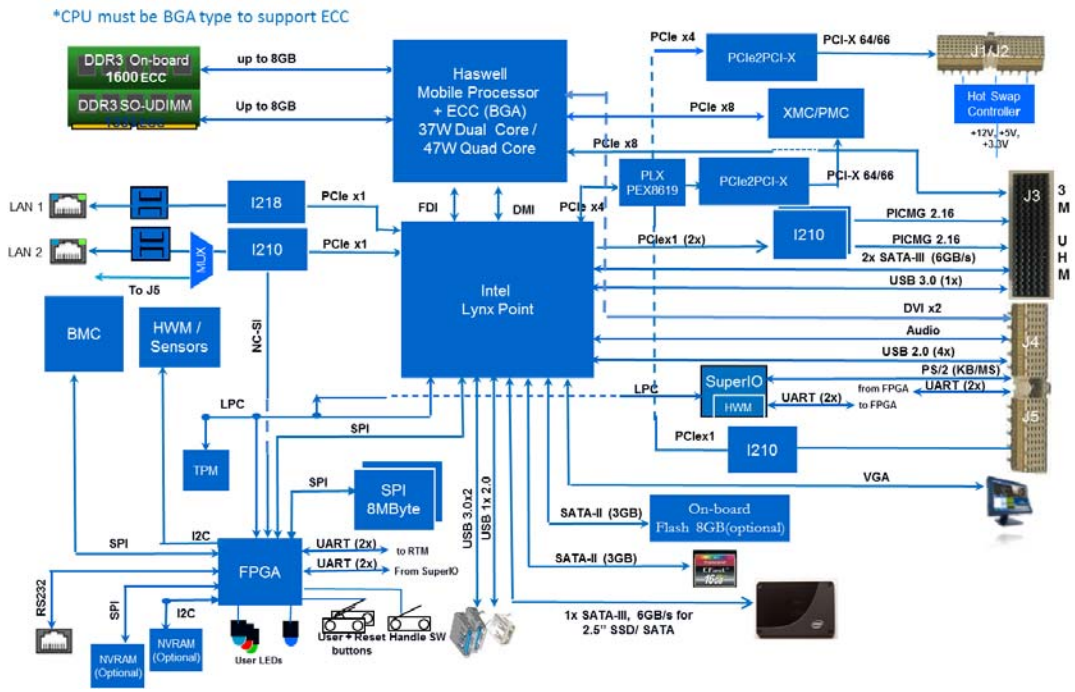


Figure 1.1 MIC-3396 functional block diagram

1.4 Jumpers and Switches

Table 1.4 and table 1.5 list the jumper and switch functions. Read this section carefully before changing the jumper and switch settings on your MIC-3396 board.

Table 1.4: MIC-3396 jumper descriptions

Number	Function
CN1	Clear CMOS
J5	Switch VGA output to front panel or to rear

Table 1.5: MIC-3396 switch descriptions

Number	Function
SW1-1	PCI Bridge Master/Drone Mode
SW1-2	Drone Mode PCI bus Reset
SW2	Front COM & RTM COM1/COM2 ports selection for BMC/SIO UART

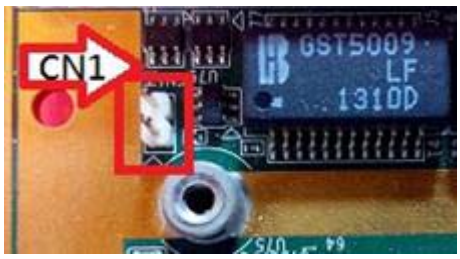
1.4.1 Clear CMOS (CN1)

This jumper is used to erase CMOS data. Follow the procedures below to clear the CMOS.

1. Turn off the system.
2. Close jumper CN1 for about 3 seconds.
3. Set jumper CN1 as Normal.
4. Turn on the system. The BIOS is reset to its default setting.

Table 1.6: CN1 Clear RTC

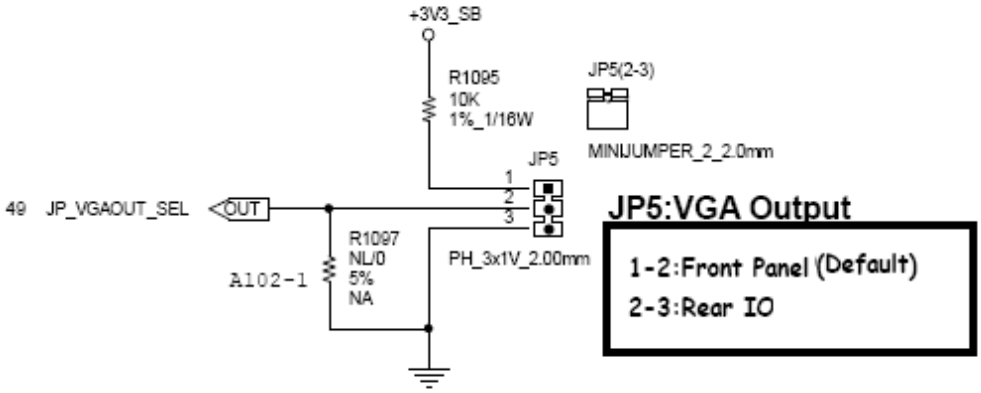
	Closed	Clear RTC
Default	Open	Normal

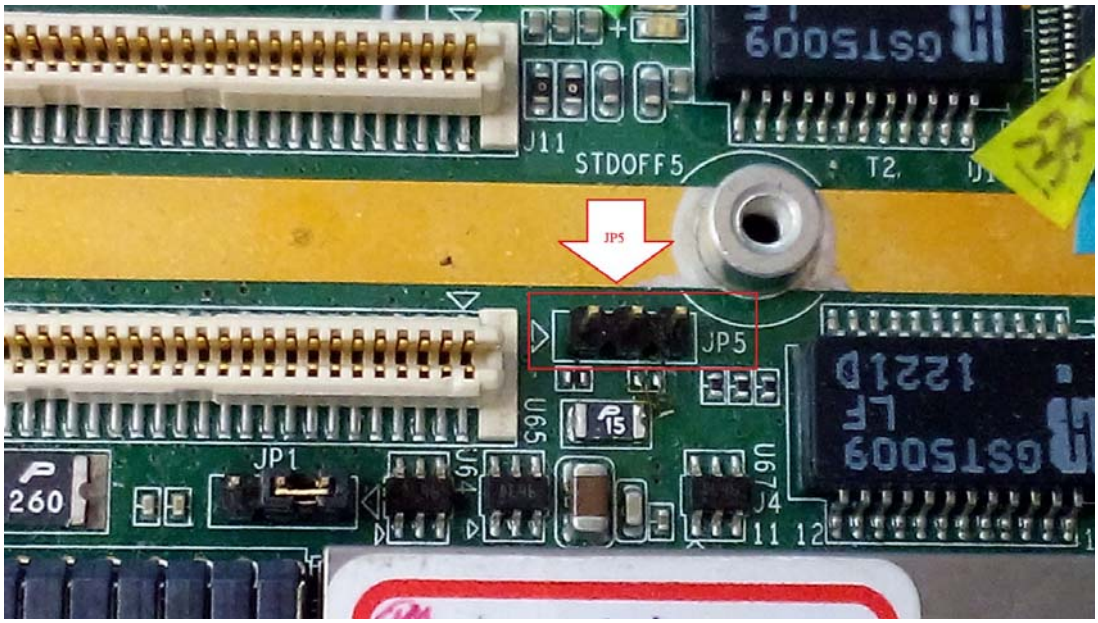


1.4.2 VGA Output (JP5)

This jumper is used to switch VGA output from front panel to rear.

Table 1.7: JP5		
Default	1-2	Front Panel
	2-3	Rear IO





1.4.3 Switch Settings

Note! ■ *represents the key*

Table 1.8: SW1-1 PCI Bridge Master/Drone Mode

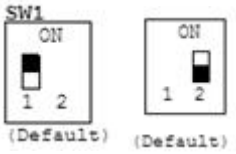
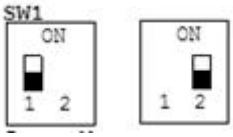
Default	Master Mode	
	Drone Mode	

Table 1.9: SW1-2 DRONE_PCISRT#_SW

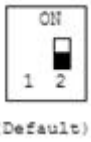
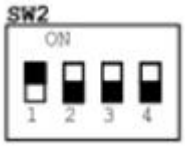
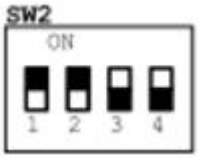
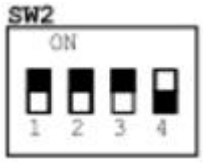
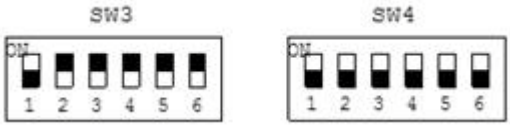
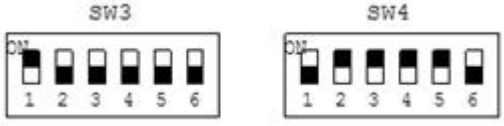
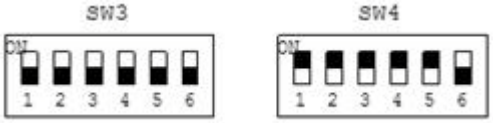
Default	Drone Mode w/o J1 RST	
	Drone Mode w/ J1 RST	

Table 1.10: SW2 Front COM & RTM COM1/COM2 ports selection for BMC/SIO UART		
Default	Front COM for BMC RTM COM1 for SIO COM1 RTM COM2 for SIO COM2	
	Front COM for SIO COM1 RTM COM1 for BMC RTM COM2 for SIO COM2	
	Front COM for SIO COM2 RTM COM1 for SIO COM1 RTM COM2 for BMC	

1.4.4 RIO-3316-C1E DIP Switch Setting

Table 1.11: SW3 & SW4 for Internal COM1		
Default	RS232	
	RS422	
	RS485	

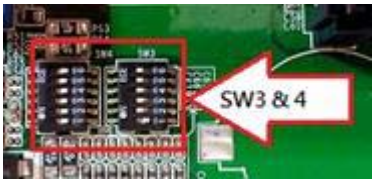
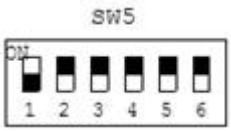
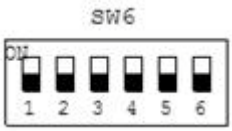
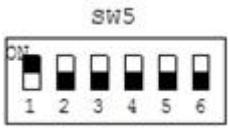
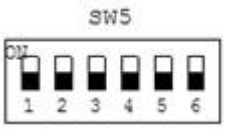
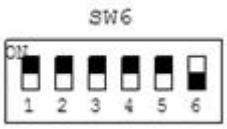
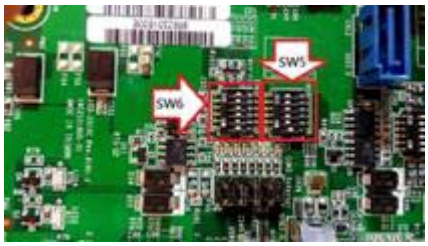


Table 1.12: SW5 & SW6 for COM2			
Default	RS232		
	RS422		
	RS485		



These switches are only available for the RIO-3316-C1E model.

1.5 Connector Definitions

Table 1.14 lists the function of each connector and Figure 1.3 and 1.4 illustrate each connector location.

Table 1.13: MIC-3396 connector descriptions

Number	Function
SATA1	SATA HDD daughter board
CFAST1	CFAST Socket
J15	XMC
SODIMM1	SODIMM socket
J1/J2	Primary CompactPCI bus
J3/J4/J5	Rear I/O transition

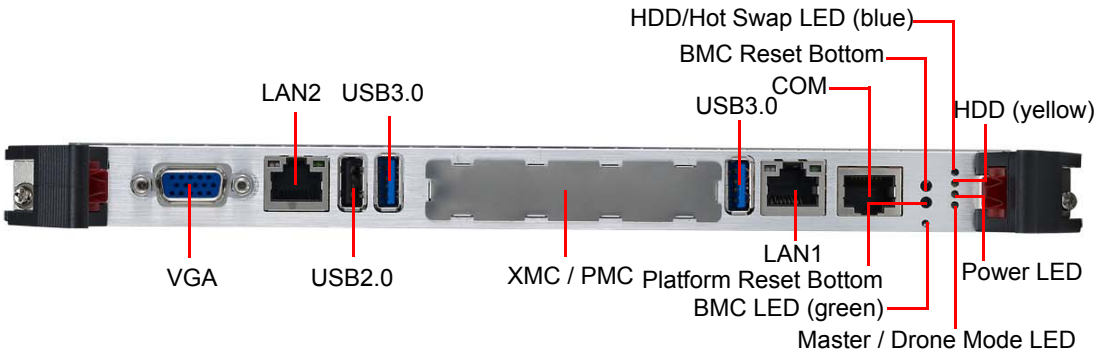


Figure 1.2 MIC-3396 Front Panel Ports, Indicators and Buttons

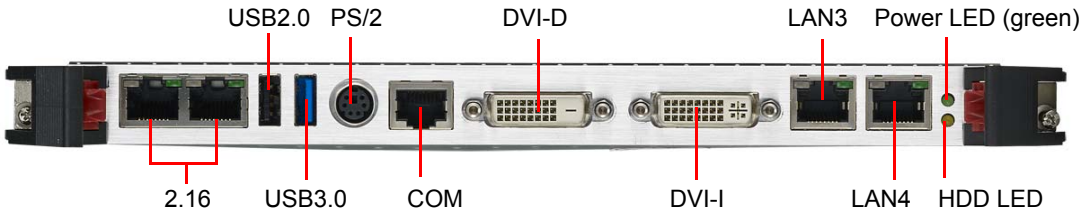


Figure 1.3 RIO-3316-C1E Front Panel Ports and Indicators

1.5.1 USB Connectors

The MIC-3396 provides up to six Universal Serial Bus (USB) 2.0 and three Universal Serial Bus (USB) 3.0 channels. Two USB 3.0 and one USB 2.0 ports are on the front panel of MIC-3396. Four other USB 2.0 and one other USB 3.0 channels are routed to rear I/O via the J3/J5 connector. One USB2.0 and one USB3.0 ports are on the front panel of RIO-3316-C1E, the other three are on-board connectors. The USB interface provides complete plug and play, hot attach/detach for up to 127 external devices. The MIC-3396 USB interface complies with USB specification R2.0 and R3.0, and is fuse protected (5 V @ 1.1 A).

1.5.2 Serial Ports

The MIC-3396 provides one serial port and the RIO-3316 provides two serial ports. The serial port is available as RS-232 interfaces via RJ-45 connectors on the front panel of MIC-3396. An RJ-45 to DB-9 adaptor cable is provided in the MIC-3396 accessories to facilitate connectivity to external console or modem devices. The BIOS Advanced Setup program covered in Chapter 2 provides a user interface for features such as enabling or disabling the ports and setting the port address. Many serial devices implement the RS-232 standard in different ways. If you have problems with a serial device, be sure to check pin assignments on Table 1.11 for the connectors. The IRQ and address range for these ports are fixed. However, if you wish to disable the port or change these parameters later, you can do this in the system BIOS setup.

1.5.3 Ethernet Configuration

The MIC-3396 is equipped with two high performances, PCI-Express based, network interface controllers which provide fully compliant IEEE802.3 10/100/1000Base-TX Ethernet interfaces; QM87 built-in PHY chip which also provides 10/100/1000Base-TX Ethernet interface. Users can choose the LAN1 and LAN2 either via the front panel RJ-45 connectors or the LAN3 and LAN4 on the rear I/O module. Furthermore, the MIC-3396 supports the PICMG 2.16 Packet Switching Backplane Specification via the J3 connector.

1.5.4 SATA Daughter Board Connector (SATA1 and Extension Module)

The MIC-3396 provides one SATA interface via SATA1 connector for either a daughter board for SATA HDD. It is optional as onboard HDD. Two SATA interfaces are connected to RTM for extra SATA HDDs request.

1.5.5 System Rest and BMC Reset Button

The MIC-3396 provides a system reset button located on the front panel. The system reset button resets all payload and application-related circuitry. It does not reset the system management (IPMI) related circuitry. A separate BMC reset button on the front panel is provided for the BMC and related hardware.

1.6 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from your CompactPCI chassis before you work on it. Don’t touch any components on the CPU board or other boards while the CompactPCI chassis is powered.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a board may damage sensitive electronic components.
- Always ground yourself to remove any static charge before you touch your CPU board. Be particularly careful not to touch the chip connectors.
- Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in its antistatic packaging when it is not installed in the chassis, and place it on a static dissipative mat when you are working with it. Wear a grounding wrist strap for continuous protection.

1.7 Installation Steps

The MIC-3396 contains electro-statically sensitive devices. Please discharge your clothing before touching the assembly. Do not touch components or connector pins. We recommend that you perform assembly at an anti-static workbench.

1.7.1 HDD Installation Steps

The MIC-3396 supports 2.5” SATA hard disk drive. The SATA HDD daughter board is assembled on the MIC-3396, but the SATA HDD brackets are not assembled on the MIC-3396. The brackets and screws are packed as accessories in the package. Following steps illustrate the installation of the SATA HDD.

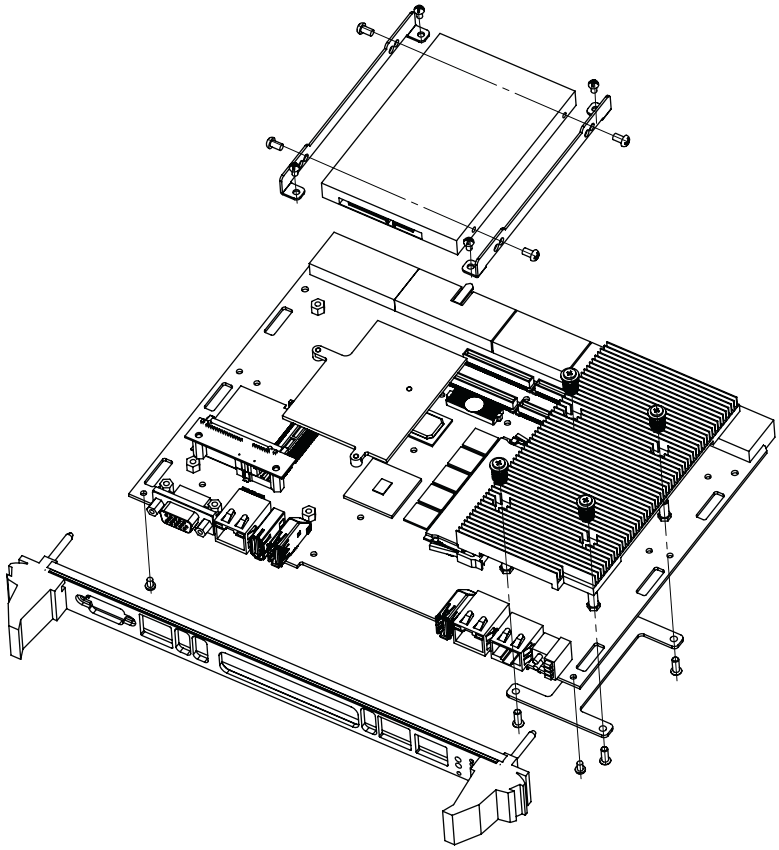


Figure 1.4 Complete assembly of MIC-3396

1. Align the HDD bracket on the side of HDD and fasten 4pcs M2.5 screw on the on the bracket.

Figure 1.5 Fasten screws on the SATA HDD bracket

2. Put the SATA HDD with bracket on the post and introduce SATA HDD into SATA connector.

Figure 1.6 Introduce SATA HDD into SATA connector

1.8 Battery Replacement

The battery model number is BR2032, a 3V, 195 mAH battery. Replacement batteries may be purchased from Advantech. When ordering the battery, please contact your local sales office to check availability.

1750199011 – BATTERY 3V/195 mAH BR2032

1.9 Software Support

Windows 7, Windows 8, Windows 2008 Enterprise R2 SP1, VxWorks 6.8/6.9 and RHEL 6.4 have been fully tested on the MIC-3396. Please contact your local sales representative for details on support for other operating systems.

Chapter 2

AMI BIOS Setup

This chapter describes how to configure the AMI BIOS.

2.1 Introduction

The AMI BIOS has been customized and integrated into many industrial and embedded motherboards for decades. This section describes the BIOS which has been specifically adapted for the MIC-3396. With the AMI UEFI BIOS Setup Utility, you can modify BIOS settings and control the special features of the MIC-3396. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter describes the basic navigation of the MIC-3396 setup screens.

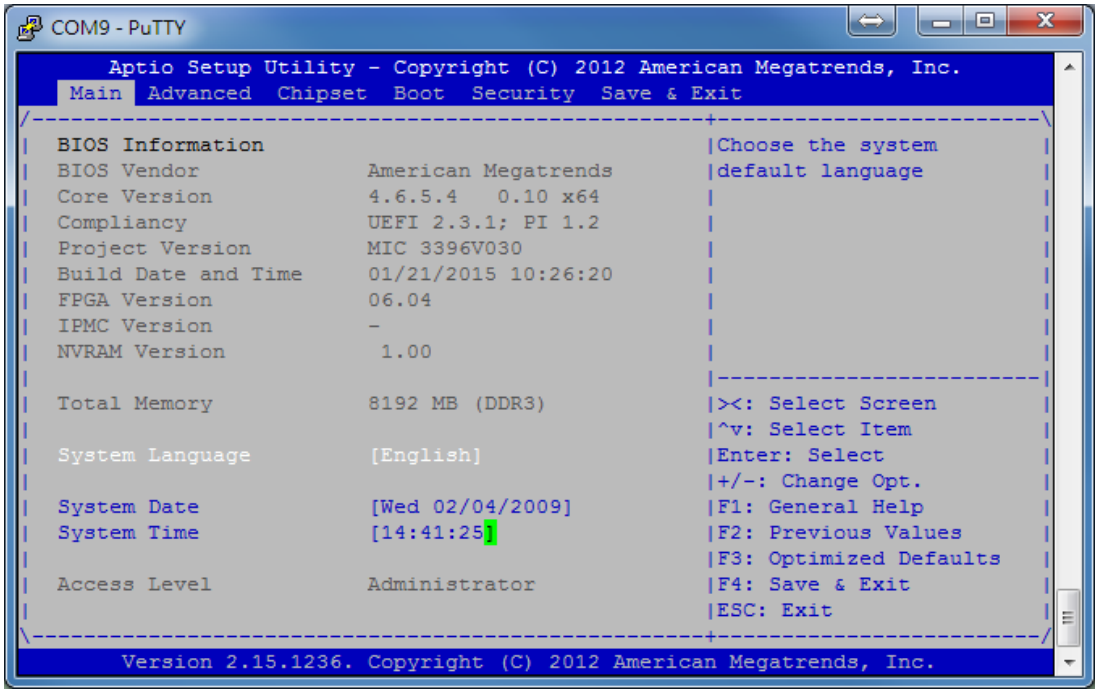


Figure 2.1 Setup program initial screen

2.2 BIOS Setup

The MIC-3396 Series system has AMI BIOS built in, with a CMOS SETUP utility that allows users to configure required settings or to activate certain system features.

The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard.

When the power is turned off, the battery on the board supplies the necessary power to preserve the CMOS RAM. But there is a CMOS backup mechanism in the MIC-3396 to protect the user's personal settings, which allows final BIOS setup information to be retained always except for date/time and user password, which are reset when CMOS battery is removed, or password only erased using the clear jumper.

When the power is turned on, press the <Del> button during the BIOS POST (Power - On Self Test) to access the CMOS SETUP screen.

Control Keys	
<↑> <↓> < → > < ← >	Move to select item
< → > < ← >	Select Screen
< ↑ > < ↓ >	Select item
<Enter>	Select
<+/->	Change Option
<F1>	General help, for Setup Sub Menu
<F2>	Previous values
<F3>	Optimized defaults
<F4>	Save & exit
<Esc>	Exit

2.3 Entering Setup

Turn on the computer, and there should be a POST (Power-On Self Test) screen that shows the BIOS supporting the CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that the CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press <DEL> and you will immediately be allowed to enter Setup.

2.3.1 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

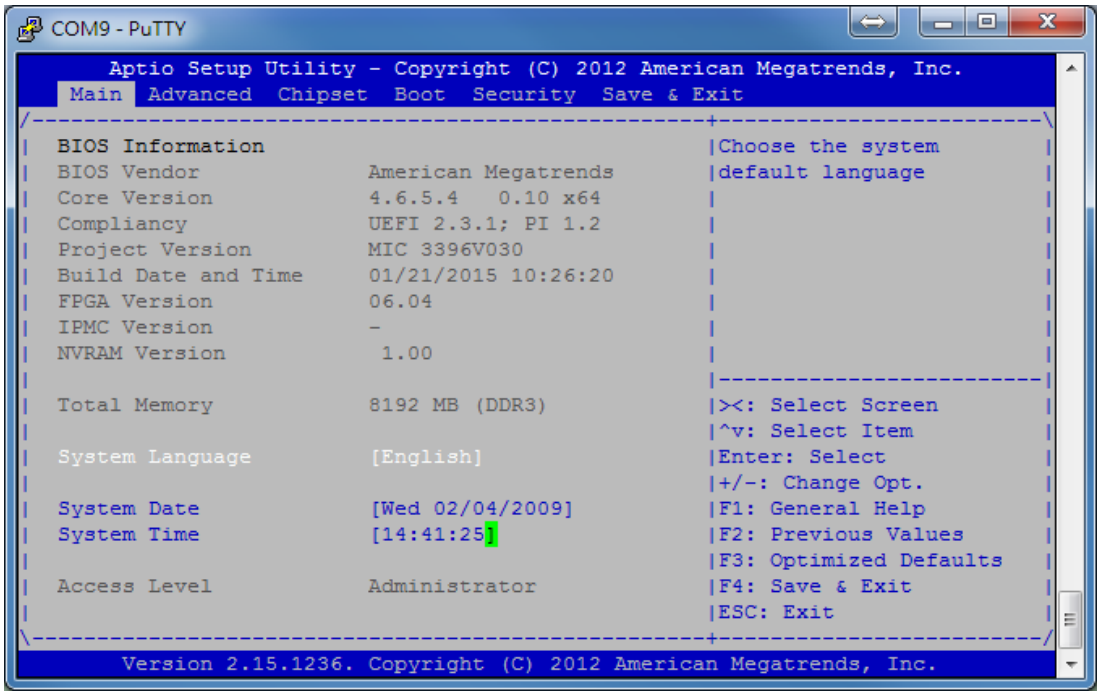


Figure 2.2 Main setup screen

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. “Grayed-out” options cannot be configured while options in blue can. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System Time/System Date**

  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

2.3.2 Advanced BIOS Features Setup

Select the Advanced tab from the MIC-3396 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub menus are described on the following pages.

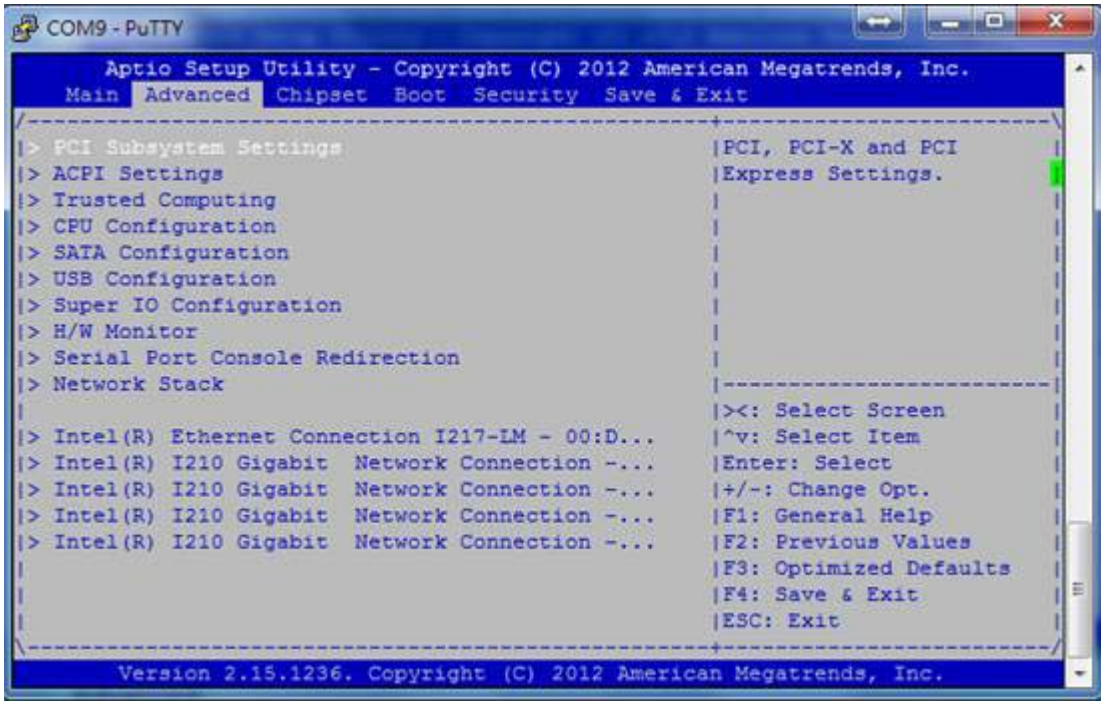
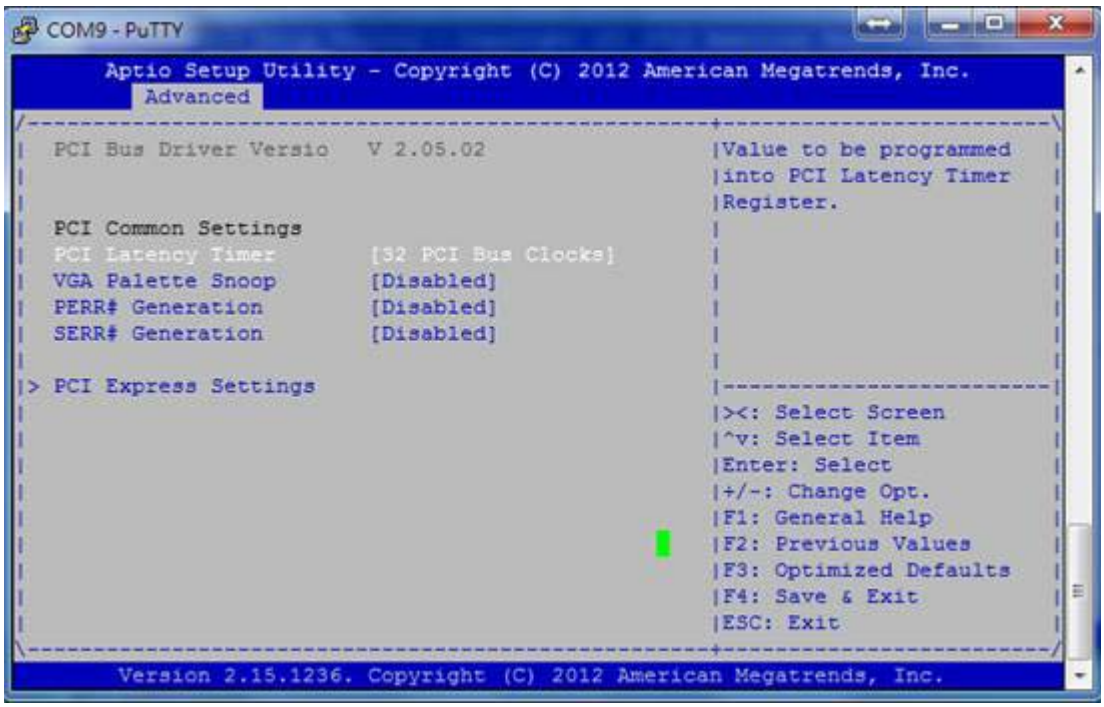


Figure 2.3 Advanced BIOS features setup screen

2.3.2.1 PCI Subsystem Setting



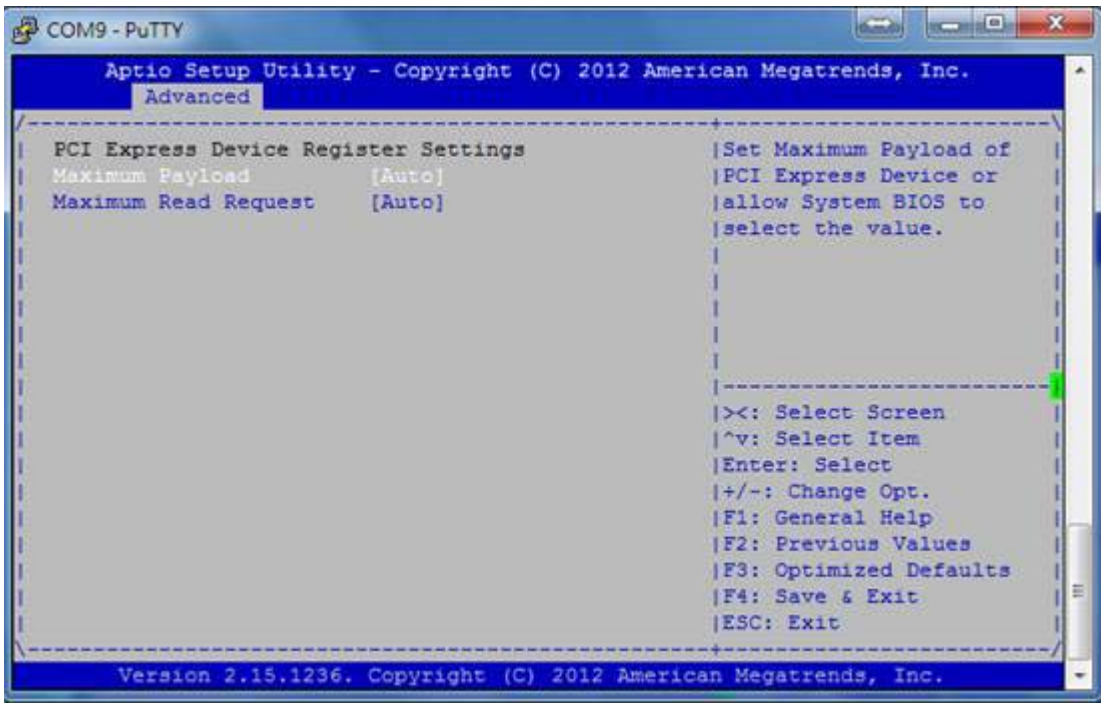


Figure 2.4 PCI Setting

- **PCI Latency Timer**
  Value to be programmed into PCI Latency Timer Register.
- **VGA Palette Snoop**
  This item allows user to enables or disables VGA Palette Register Snooping.
- **PCI Express Settings**
  Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.
- **Maximum Payload**
  Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.
- **Maximum Read Request**
  Set Maximum Read Request Size of PCI Express Device or allow system BIOS to select the value.

2.3.2.2 ACPI Setting

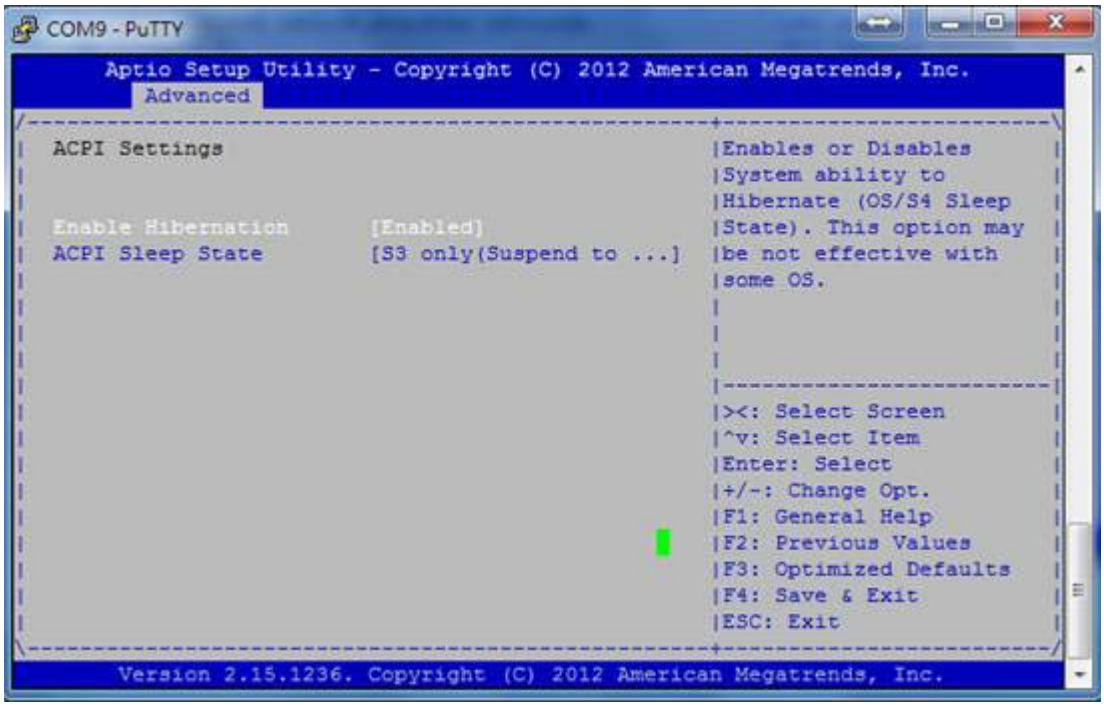


Figure 2.5 ACPI Settings

System ACPI Parameters

- **Enable Hibernation**
  Enable or Disable System Hibernation (OS/S4 Sleep State). This option may be not effective with some OS.
- **ACPI Sleep State**
  Select the ACPI sleep state the system will enter when the SUSPEND button is pressed.

2.3.2.3 Trusted Computing

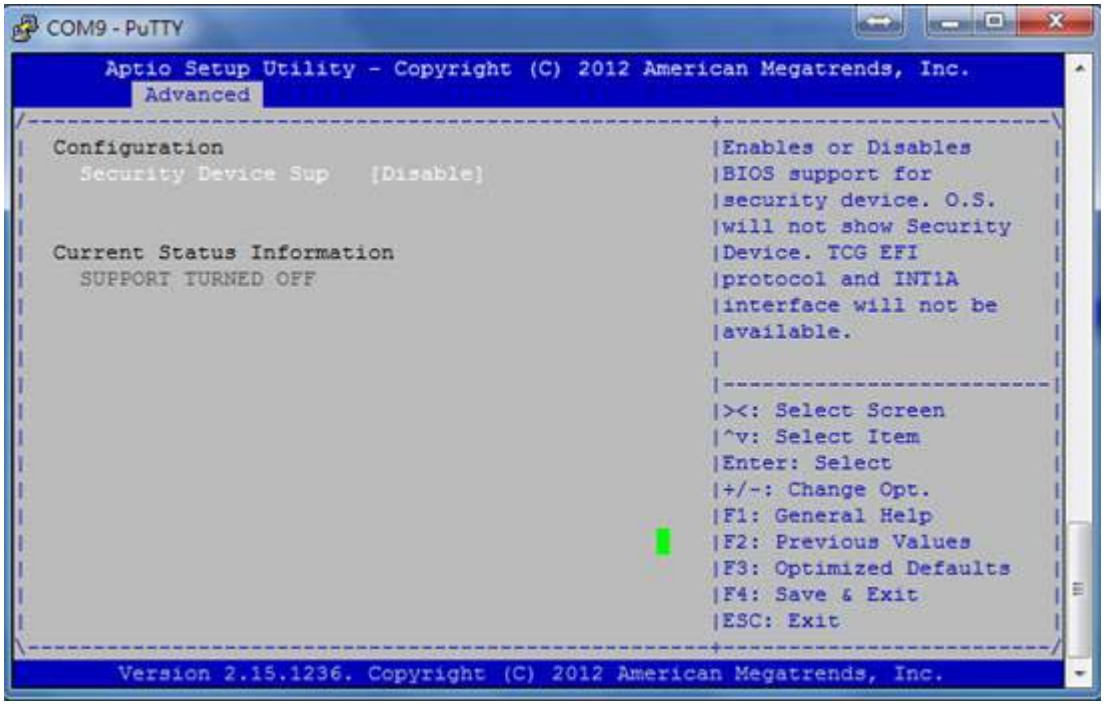


Figure 2.6 Trusted Computing

Trusted Computing settings

- **Enable/Disable Trusted Computing**
  Enables or Disables BIOS support for security device. OS will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

2.3.2.4 CPU Configuration

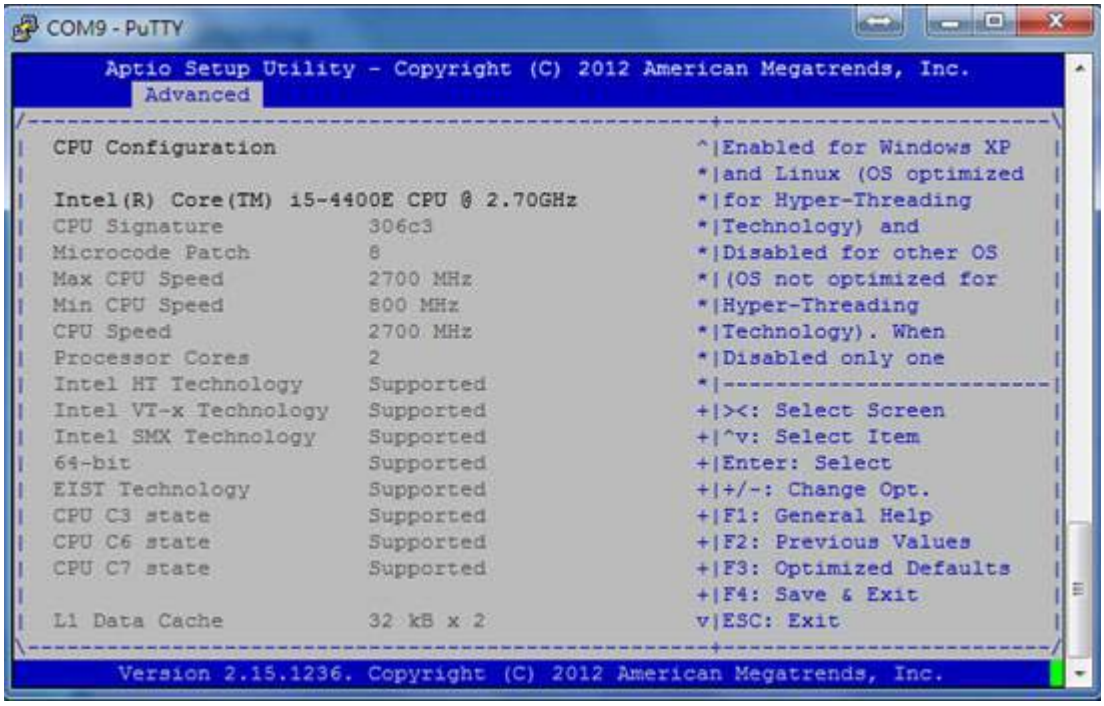


Figure 2.7 CPU configuration

- **Hyper-Threading**

  This item allows you to enable or disable Intel® Hyper Threading technology.

- **Active Processor Cores**

  It allows you to choose the number of CPU cores to activate in each processor package.

- **Limit CPUID Maximum**

  This item allows you to limit CPUID maximum value.

- **Execute Disable Bit**

  This item allows you to enable or disable the No-Execution page protection technology.

- **Intel Virtualization**

  Intel Virtualization Technology (Intel VT) is a set of hardware enhancements to Intel server and client platforms that provide software-based virtualization solutions.

  Intel VT allows a platform to run multiple operating systems and applications in independent partitions, allowing one computer system to function as multiple virtual systems.

- **Hardware Prefetcher**

  The processor fetches data and instructions from the memory into the cache are likely to be required in the near future. This reduces the latency associated with memory reads.

- **Adjacent Cache Line Prefetcher**

  This item allows users to enable or disable the adjacent cache line prefetcher feature.

- **EIST**

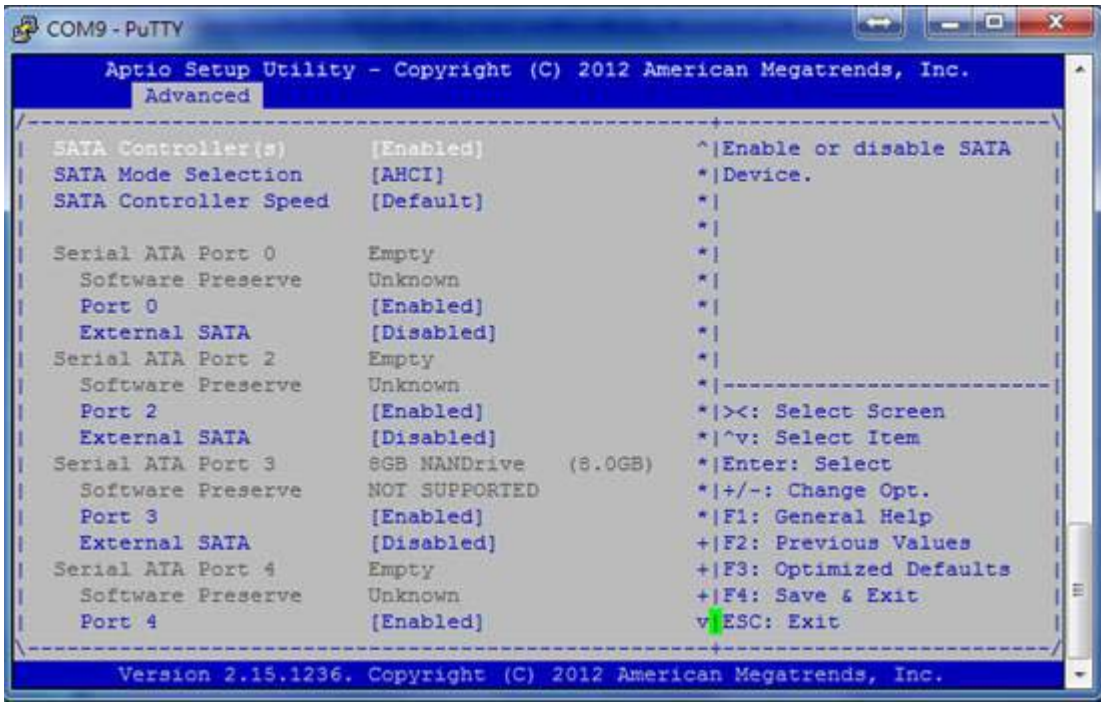
  This item allows users to enable or disable Intel SpeedStep.

- **CPU C States**

  This item allows users to enable or disable CPU C states.

- **Intel TXT(LT) support**
  Enables or Disables Intel® TXT (LT) support.

2.3.2.5 SATA Configuration



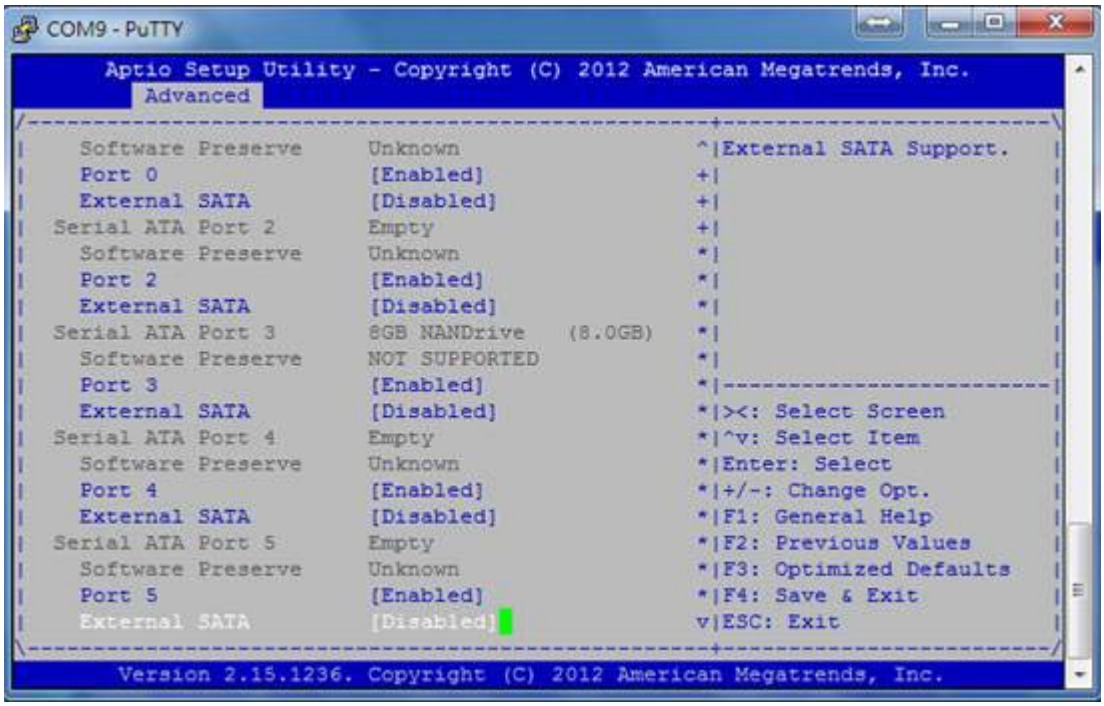


Figure 2.8 SATA configuration

- **SATA Controller**
  This items allow users to enable or disable SATA function.
- **[Disabled]**
  Disable SATA function.

- **SATA Mode Selection**

  This item allows users to determine how SATA controller(s) operate. It can be configured as IDE, AHCI or RAID mode.

- **IDE mode**

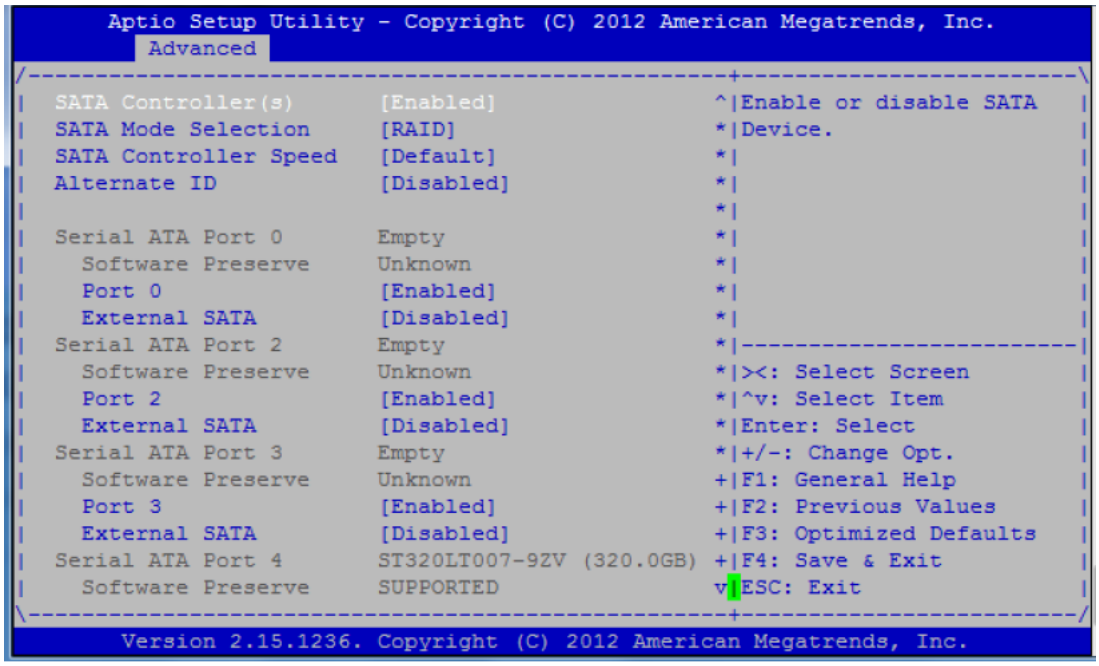
  Set to [IDE mode] when you want to use the serial ATA hard disk drives as Parallel ATA physical storage devices.

- **ACHI mode**

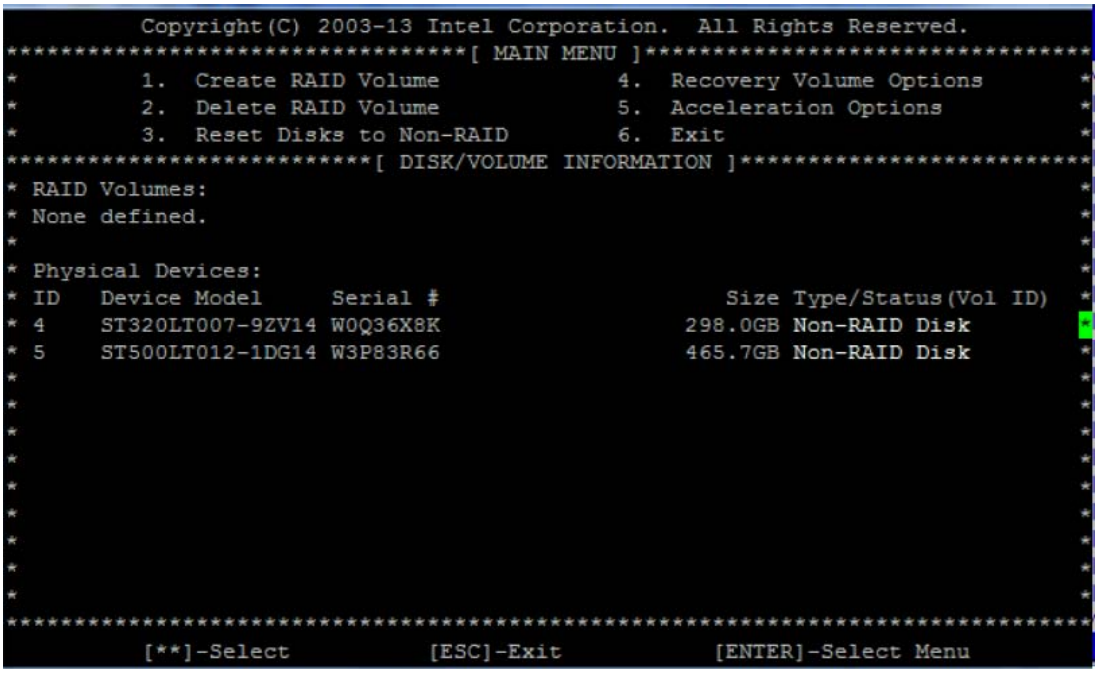
  Set to [AHCI mode] when you want the SATA hard disk drives to use the AHCI (Advanced Host Controller Interface). The AHCI allows the onboard storage driver to enable advanced serial ATA features that increase storage performance on random workloads by allowing the drive to internally optimize the order of commands.

- **RAID mode**

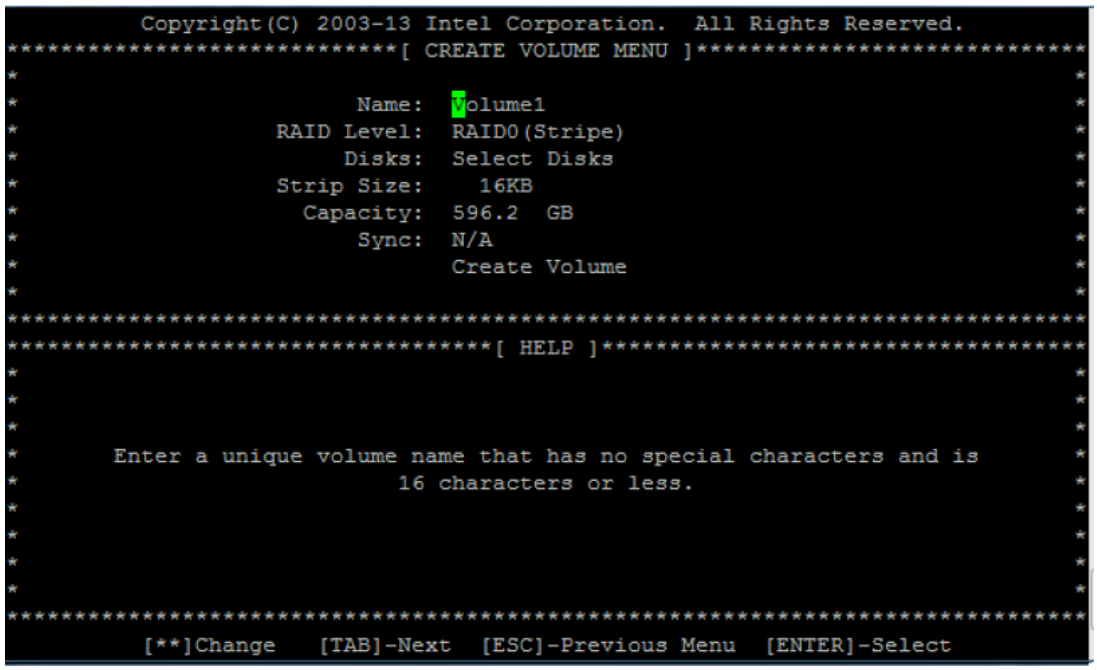
  Set to [RAID mode] when you want the SATA hard disk drives to use the RAID mode. The Intel RAID function allows the user to build up RAID0 or RAID1.



Press "Ctrl + I" into Intel® Rapid Storage Technology - Option ROM



Choose "Create RAID Volume" to build RAID0 or RAID1.



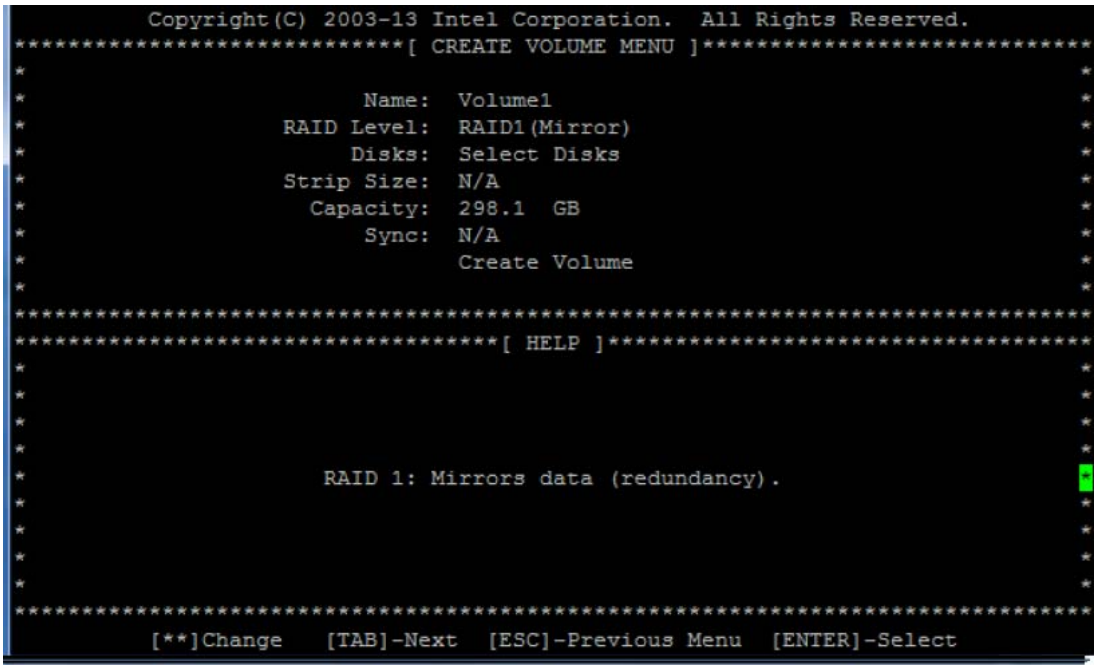


Figure 2.9 RAID mode

2.3.2.6 USB Configuration

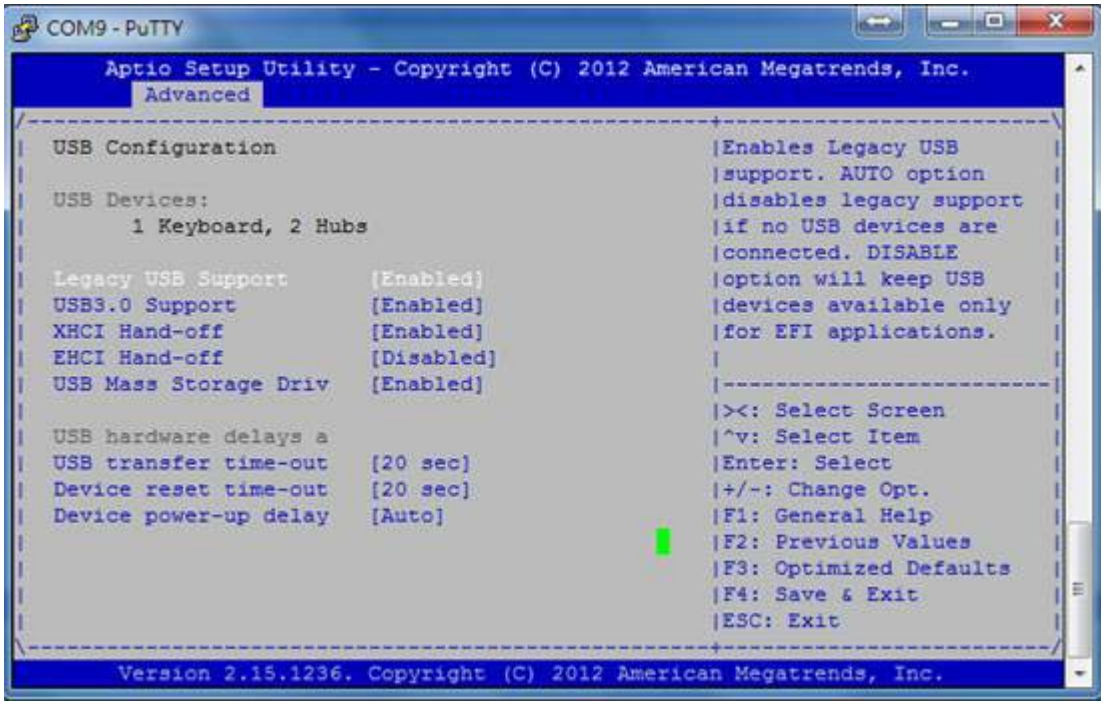


Figure 2.10 USB configuration

- **Legacy USB Support**
  Enables support for legacy USB. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB device available only for EFI applications
- **USB3.0 support**
  Enable or disable USB3.0 (XHCI) Controller support
- **XHCI Hand-off**
  This is a workaround for OSes without XHCI hand-off support.

- **EHCI Hand-off**
  This is just a workaround item under OS without EHCI hand-off support.
- **USB Mass Storage Drive**
  Enable or disable USB Mass Storage Driver Support.
- **USB transfer time-out**
  The time-out value for Control, Bulk, and Interrupt transfers.
- **Device reset time-out**
  USB mass storage device start unit command time out.
- **Device power-up delay**
  Maximum time the device will take before it properly reports itself to the host controller.

2.3.2.7 Super I/O Configuration

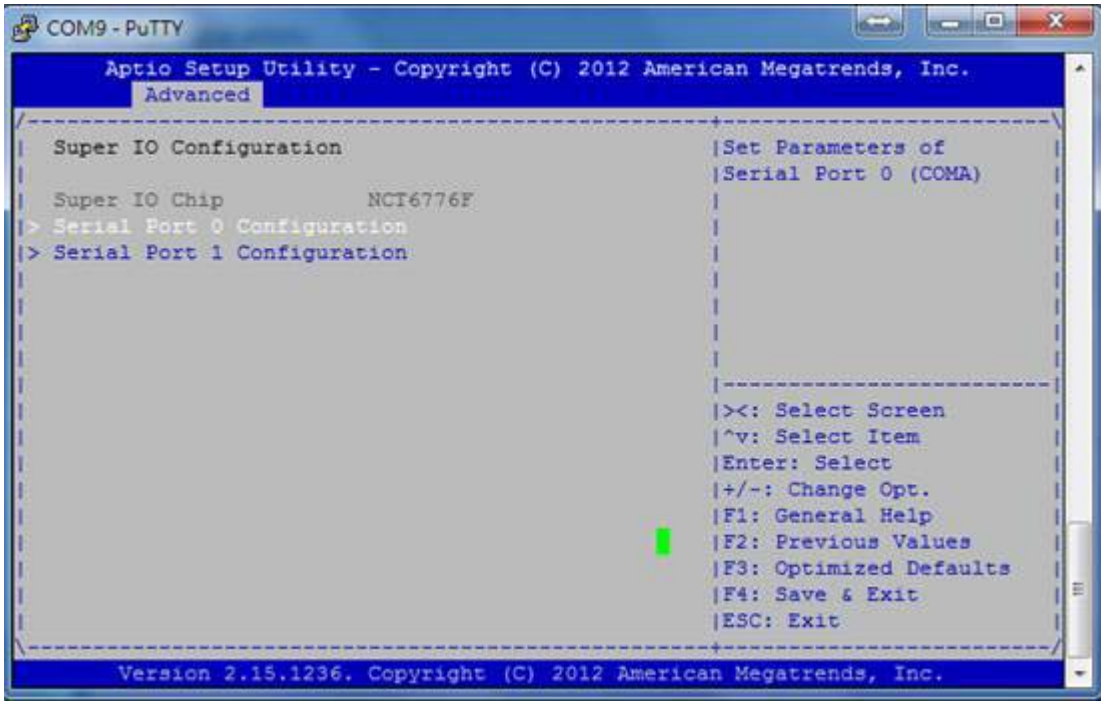
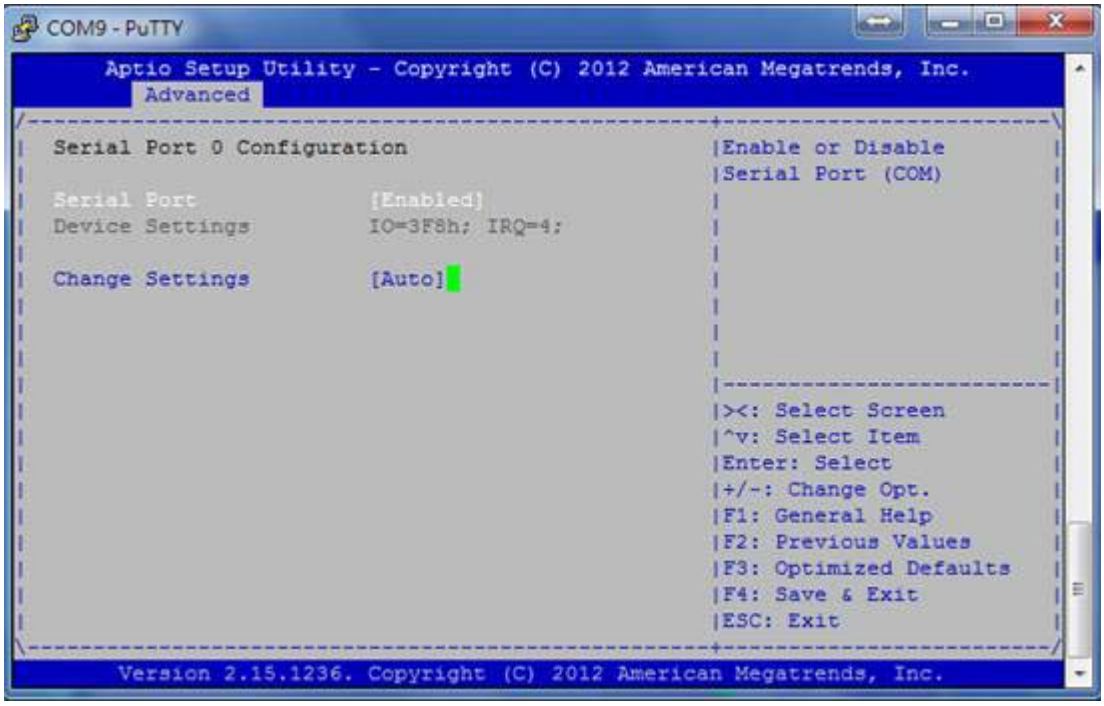


Figure 2.11 Super IO Configurations

- **Serial Port 0/1 Configuration**

  For serial port 0/1, IRQ/IO mode resource configuration, users can choose IRQ, IO and MODE.



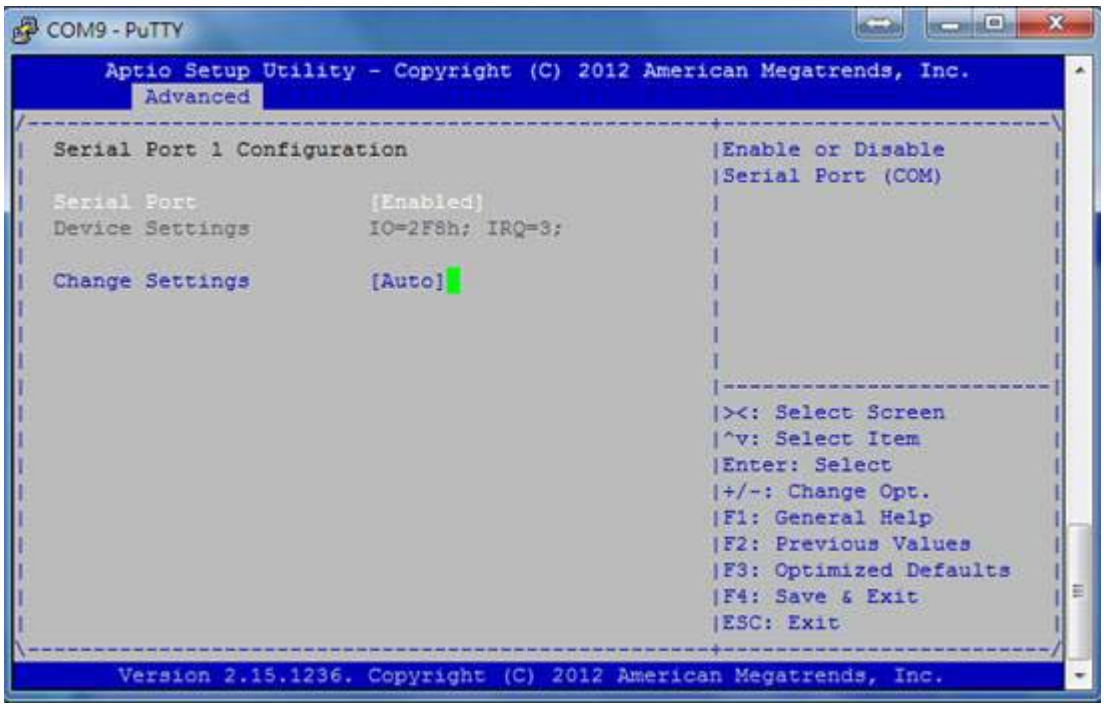


Figure 2.12 Serial Port 0/1 Configurations

2.3.2.8 H/W Monitor Configuration

System temperature, CPU temperature and voltage status can be checked in PC Health Status.

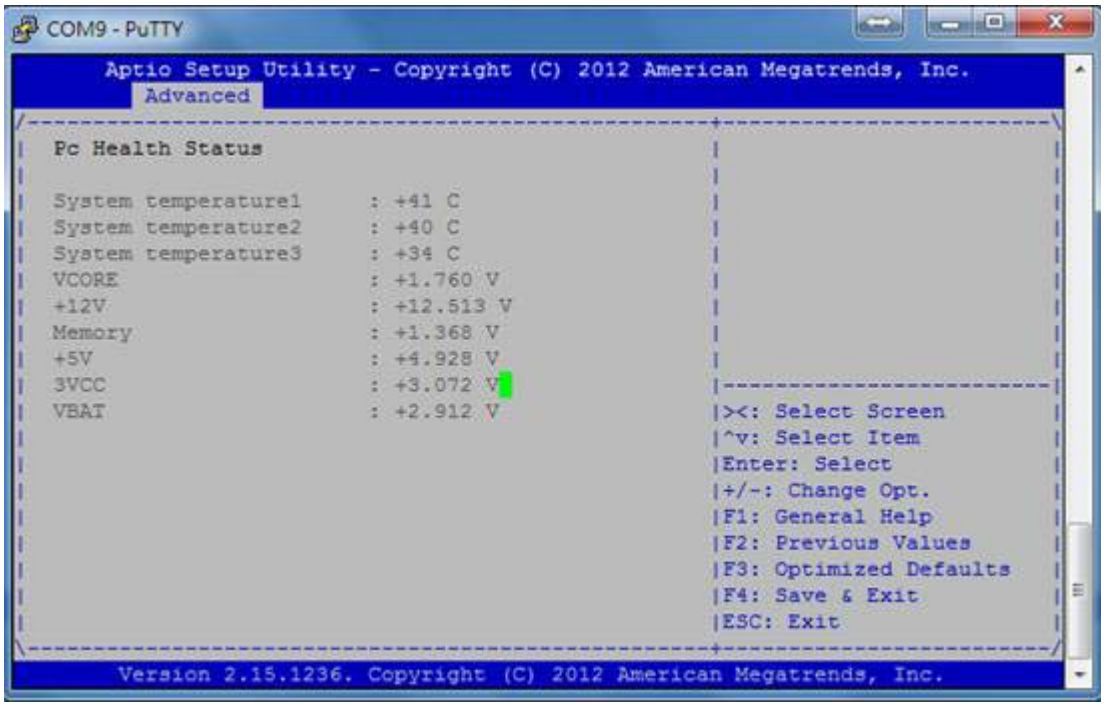


Figure 2.13 PC Health Status

2.3.2.9 Serial Port Console Redirection Setting

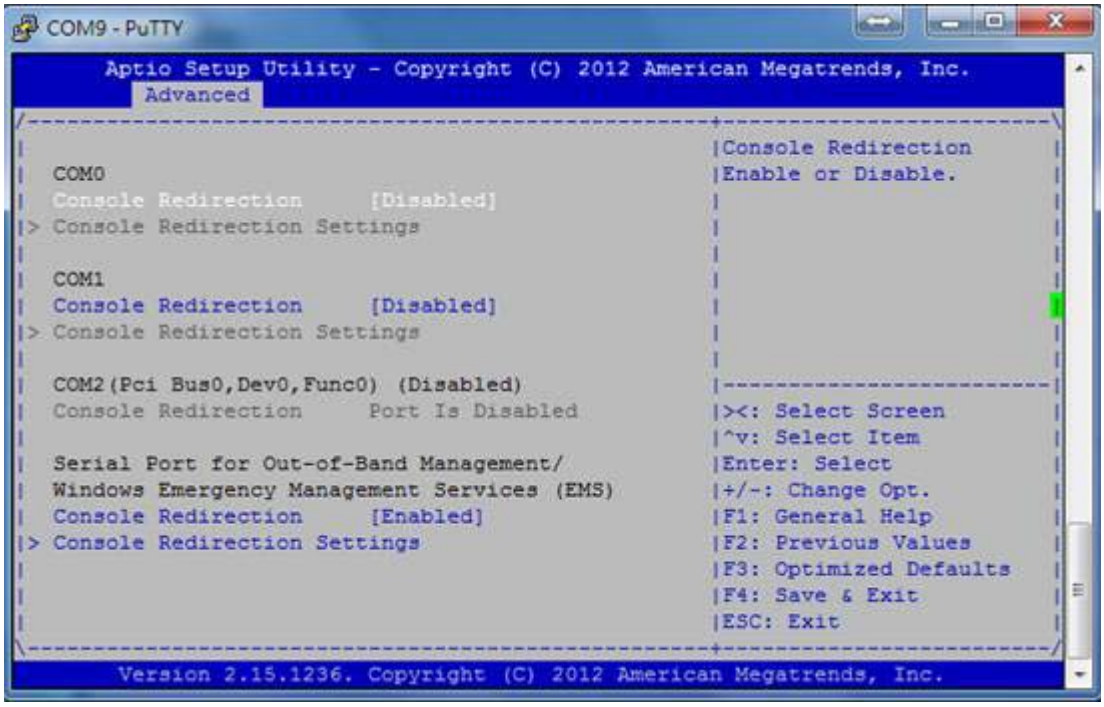


Figure 2.14 Console redirection Settings

- **Console Redirection Settings**

  This item allows users to enable or disable console redirection or Microsoft Windows Emergency Management Services (EMS).

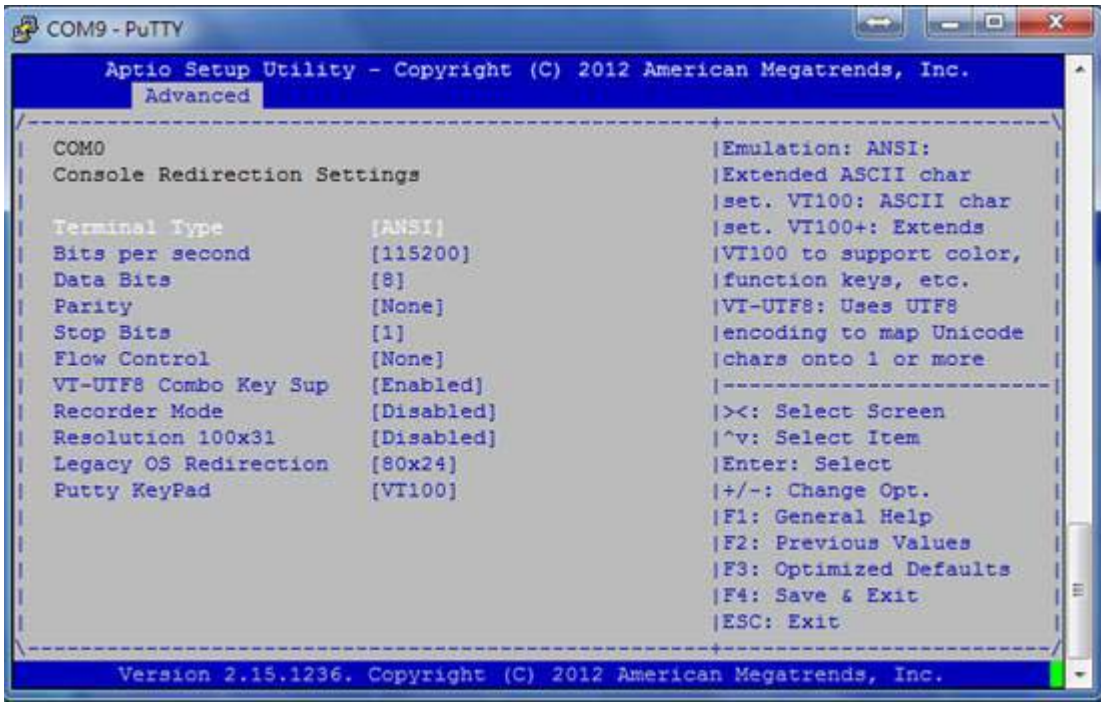


Figure 2.15 Out-of-Band Mgmt Port

- **Out-of-Band Mgmt Port**

  Select the port for Microsoft Windows Emergency Management Services (EMS) to allow for remote management of a Windows Server OS.

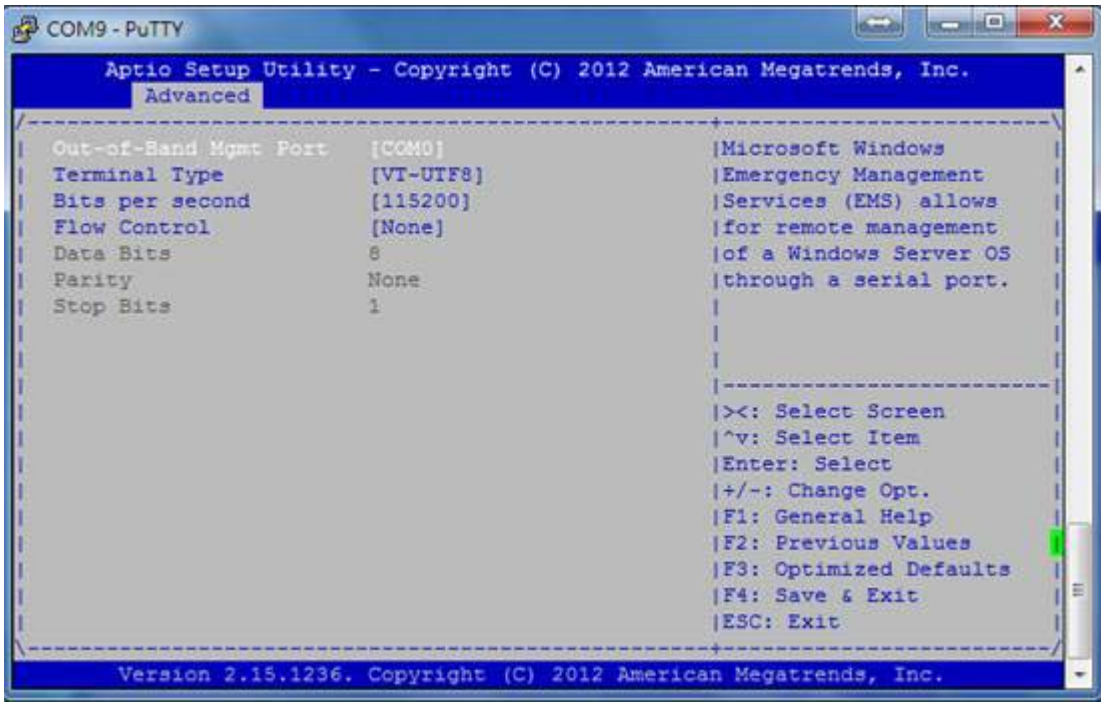


Figure 2.16 Terminal Type

- **Terminal Type**

  VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

2.3.2.10 Network Stack

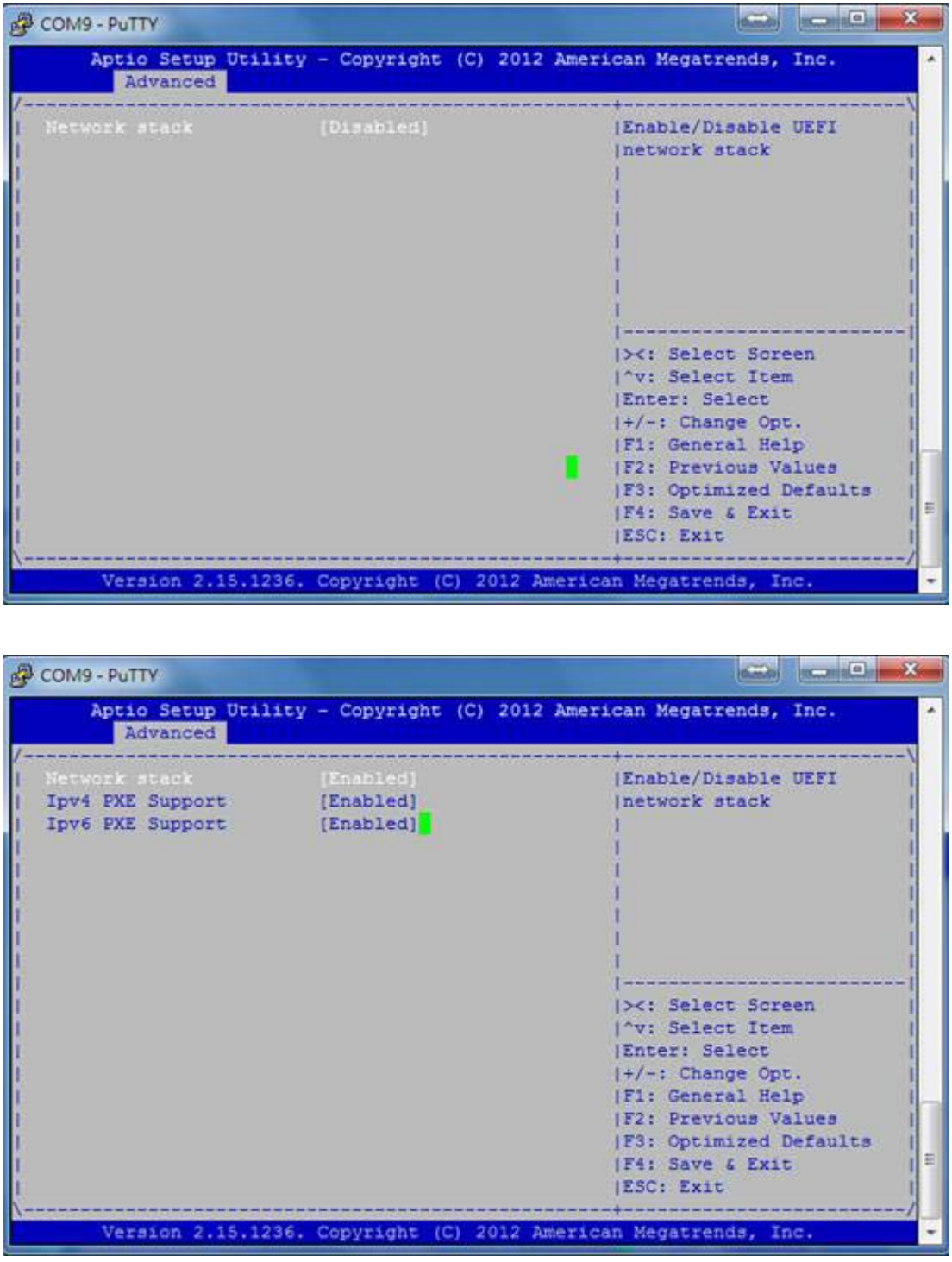


Figure 2.17 Network Stack

- **Network Stack**
  This item allows users to enable or disable UEFI network stack.

2.3.2.11 Intel ® Ethernet Connection I217-LM

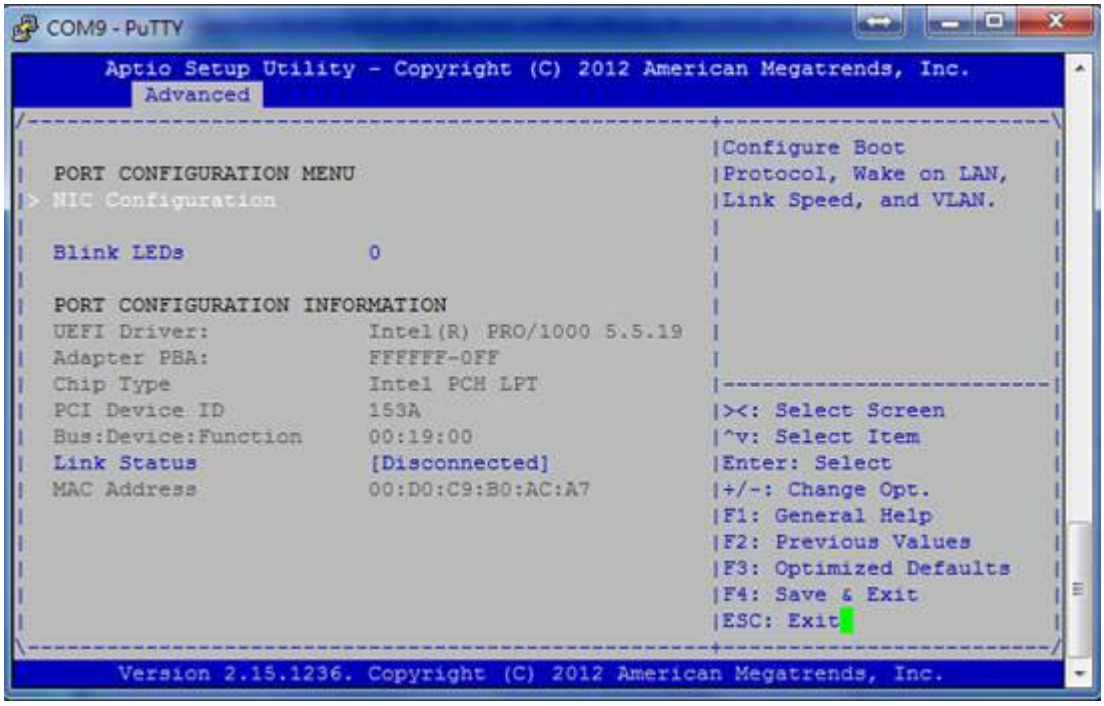


Figure 2.18 NIC Configuration Settings

- **NIC Configuration**
  Configure Boot Protocol, Wake on LAN, Link Speed, and VLAN.

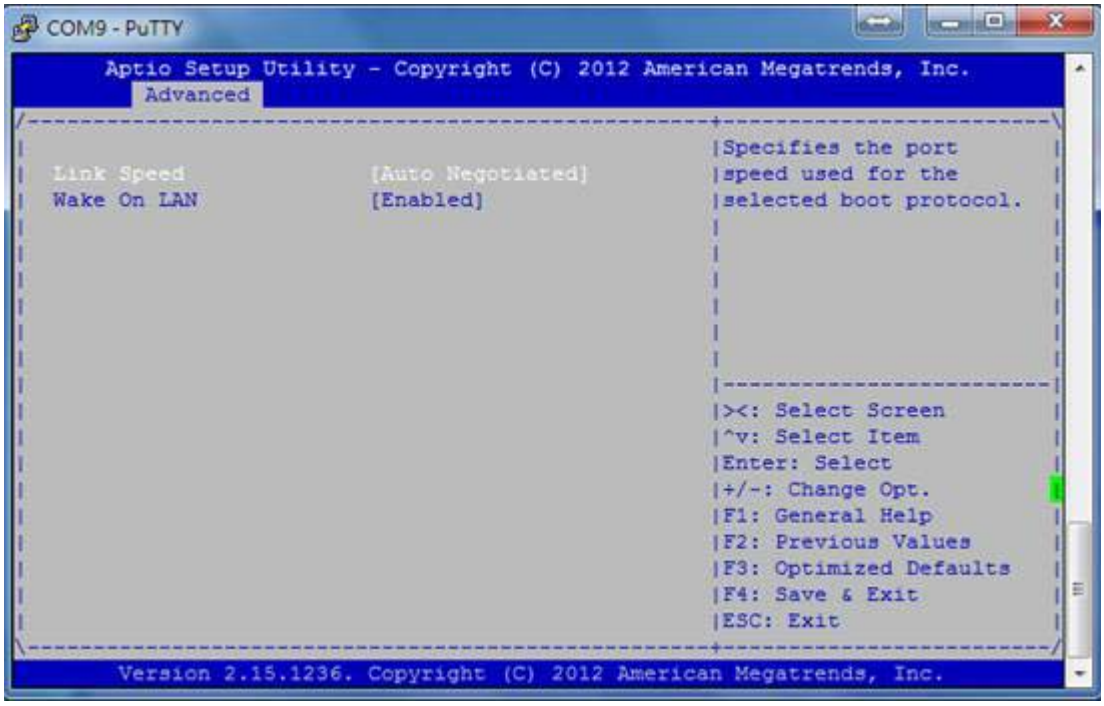


Figure 2.19 Link Speed

- **Link Speed**
  Specifies the port speed used for the selected boot protocol.
- **Wake On LAN**
  This item allows users to enable the server to be powered on.

2.3.2.12 Intel® I210 Gigabit Network Connection

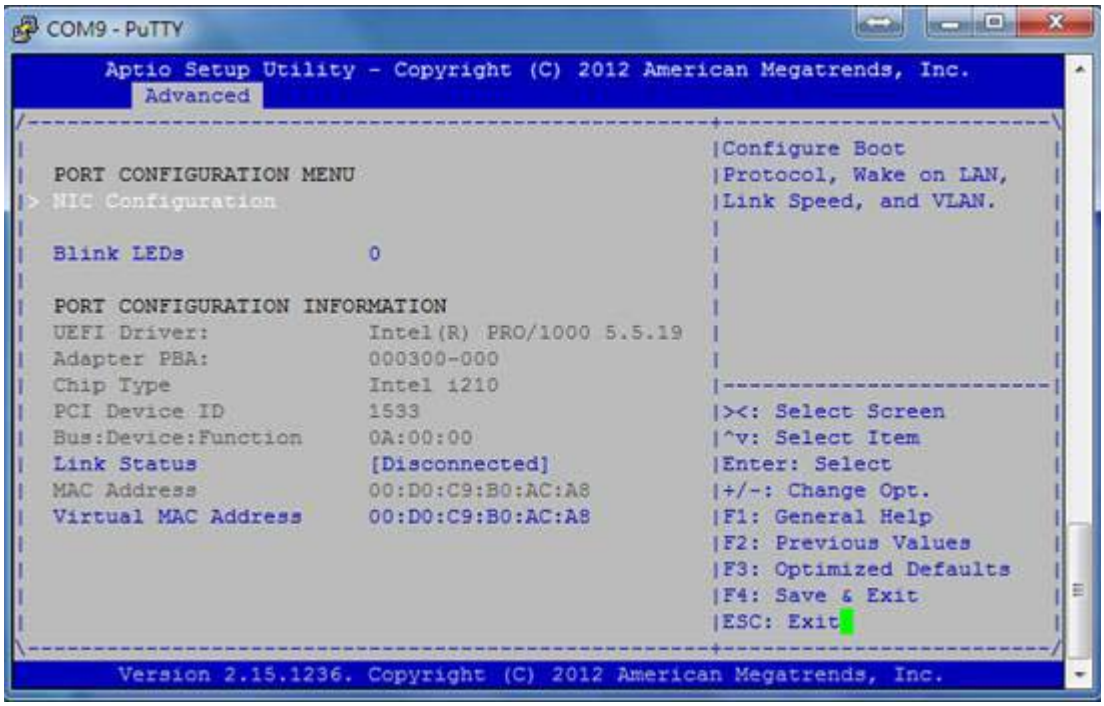


Figure 2.20 NIC Configuration Settings

- **NIC Configuration**
  Configure Boot Protocol, Wake on LAN, Link Speed, and VLAN.

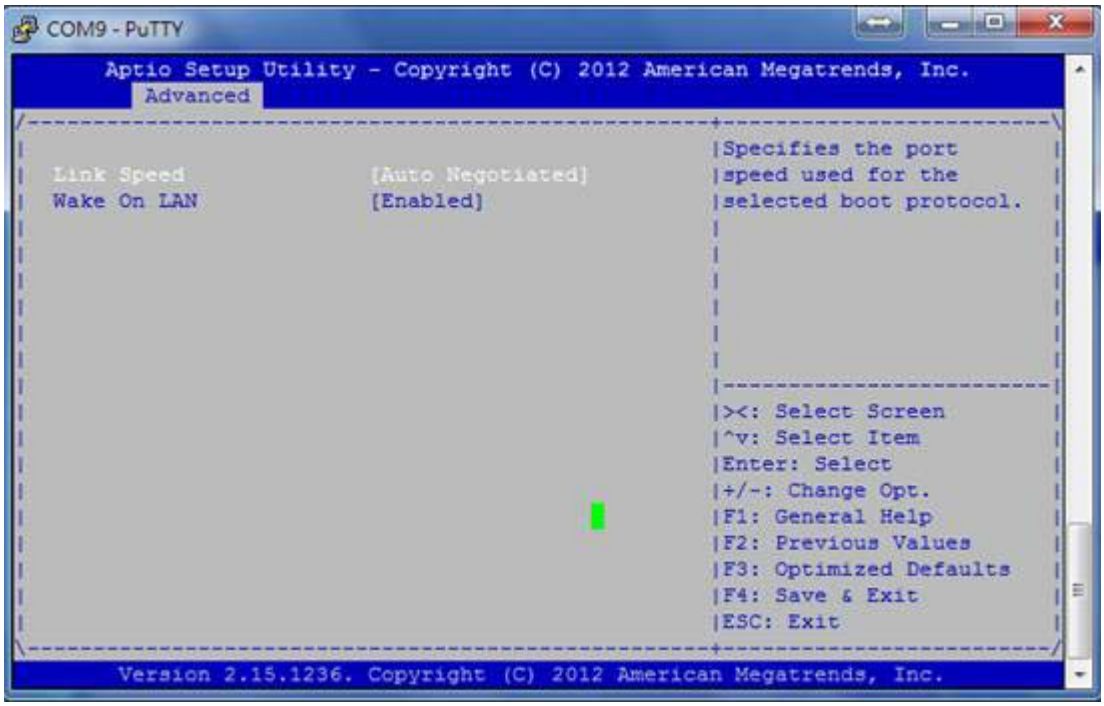


Figure 2.21 Link Speed

- **Link Speed**
  Specifies the port speed used for the selected boot protocol.
- **Wake On LAN**
  This item allows users to enable the server to be powered on.

2.3.3 Chipset Configuration Setting

Select the chipset tab from the BIOS setup screen to enter the Chipset Setup screen.

Users can select any item in the left frame of the screen to go to the sub menu for that item. Users can display a Chipset Setup option by highlighting it using the <Arrow> keys. All Chipset Setup options are described in this section. The Chipset Setup screens are shown below. The sub menus are described on the following pages.

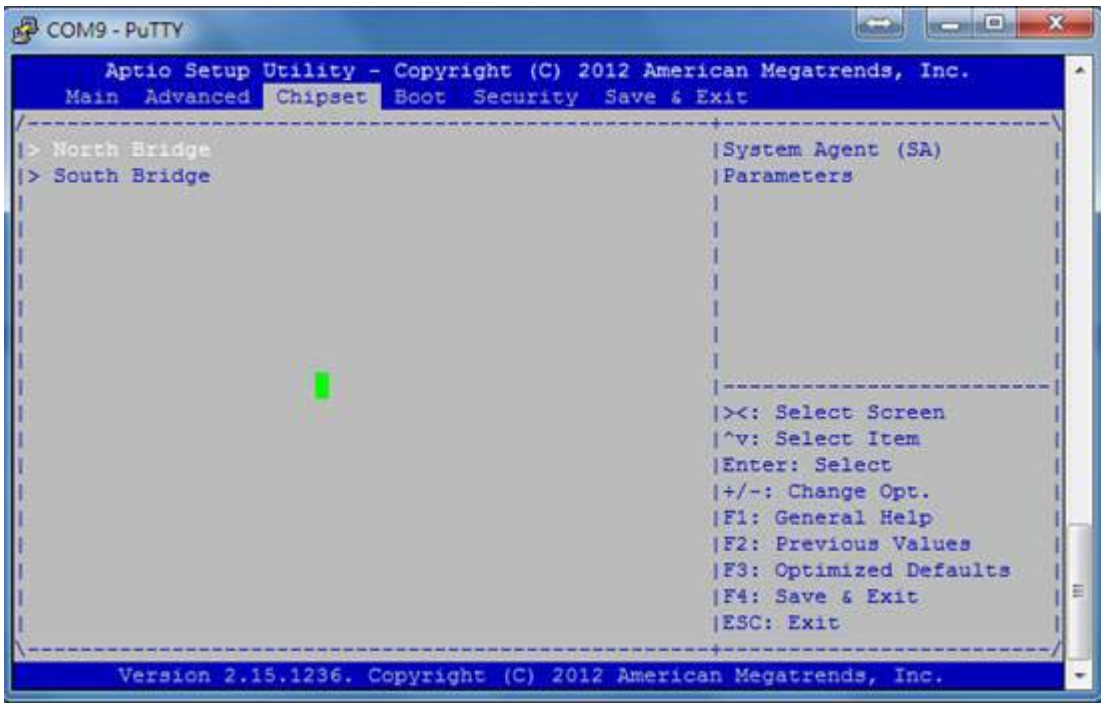


Figure 2.22 Chipset Configuration Settings

2.3.3.1 North Bridge Configuration

- **VT-d Capability**

Figure 2.23 VT-d

– **VT-d**

This item allows users to enable or disable VT-d.

- **Graphics Configuration**

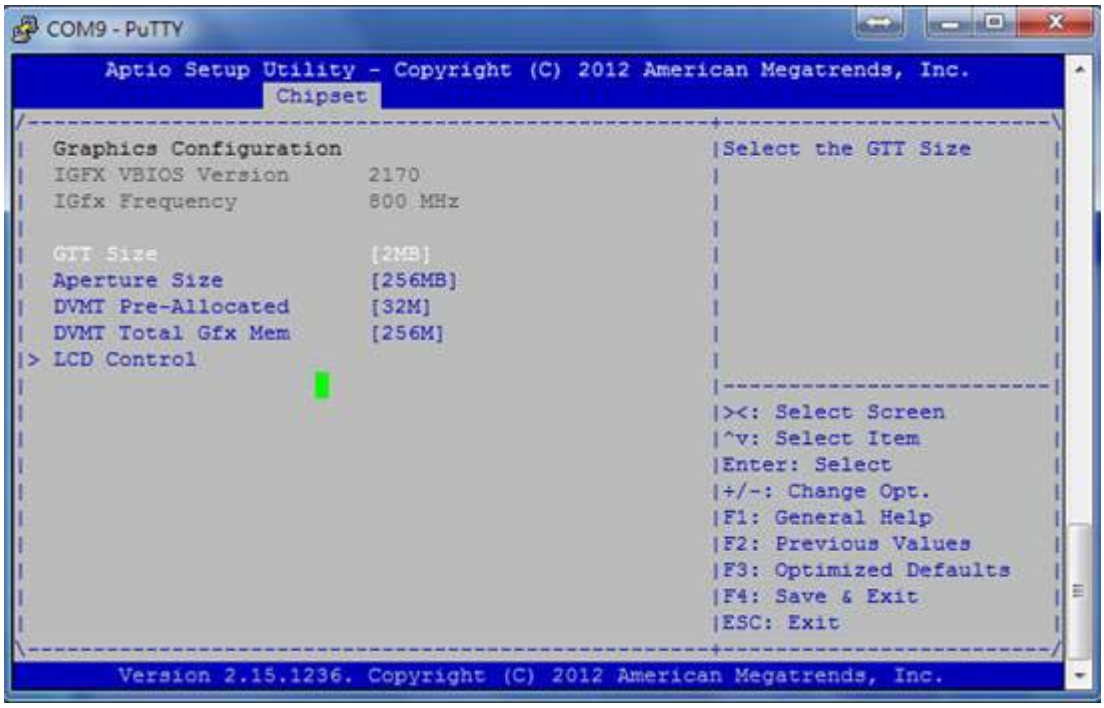


Figure 2.24 Graphics Configuration

– **GTT Size**

This item allows users to select the GTT Size.

– **Aperture Size**

This item allows users to select the Aperture Size.

– **DVMT Pre-Allocated**

This item allows users to select DVMT 5.0 Pre-Allocated (fixed) Graphics memory size used by the internal graphics device.

– **DVMT Total Gfx Mem**

This item allows users to select DVMT5.0 total Graphic memory size used by the internal graphic device.

LCD Control

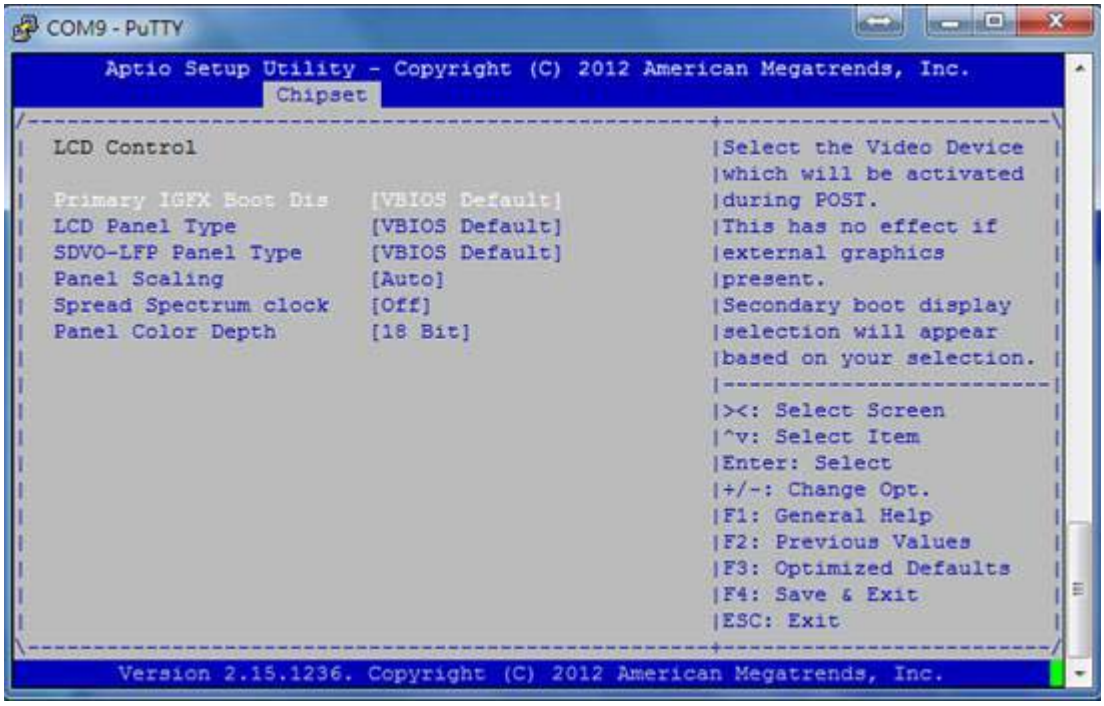


Figure 2.25 LCD Control

– **Primary IGFX Boot Dis**

This item allows users to select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection.

– **LCD Panel Type**

This item allows users to select panel resolution.

– **Panel Scaling**

This item allows users to enable or disable panel scaling.

- **NB PCIe Configuration**

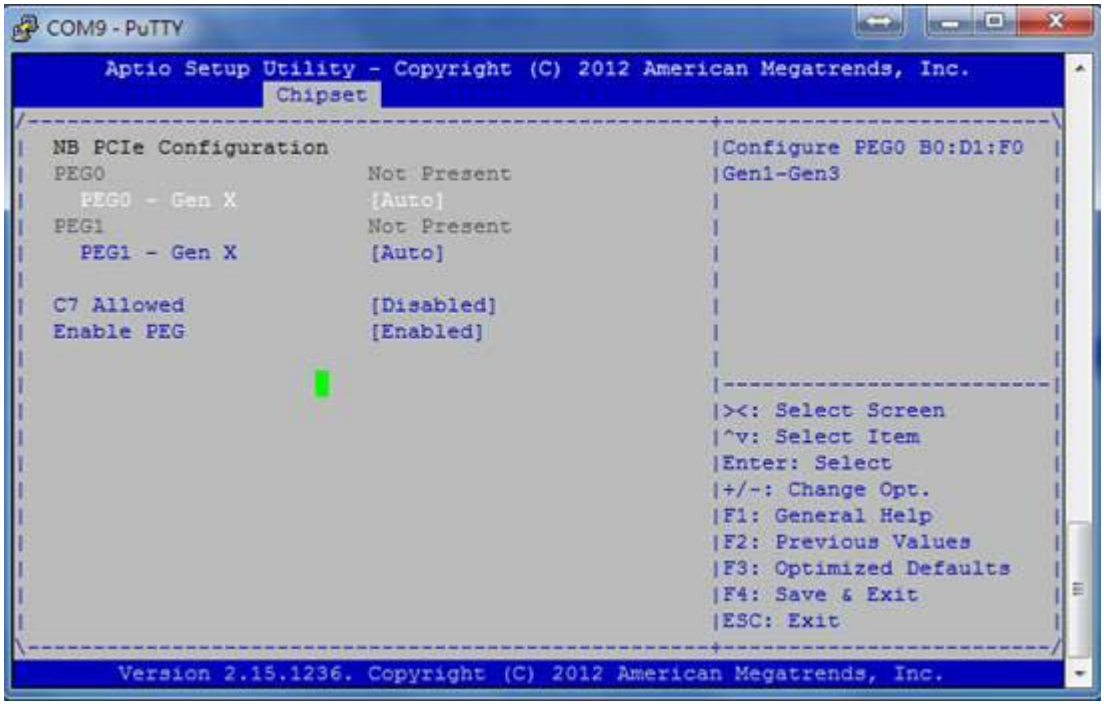


Figure 2.26 NB PCIe Configuration

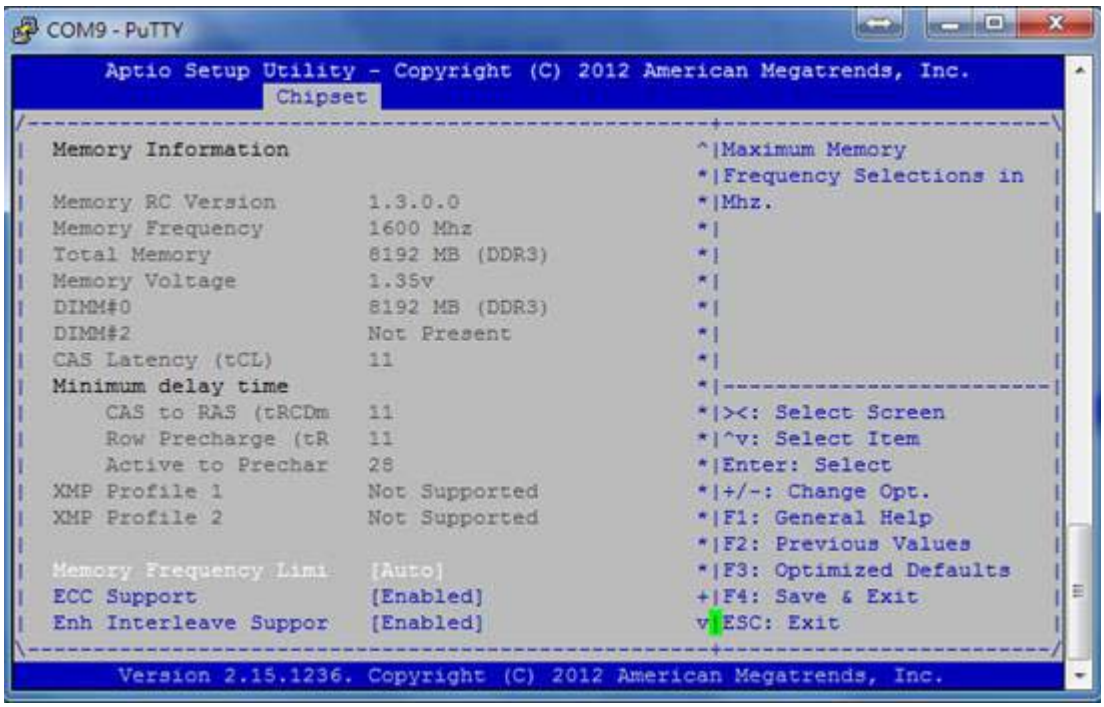
– **PEG0 - Gen x**

Select PEG0 speed.

– **Enabled PEG**

This item allows users to enable or disable PEG.

- **Memory Configuration**



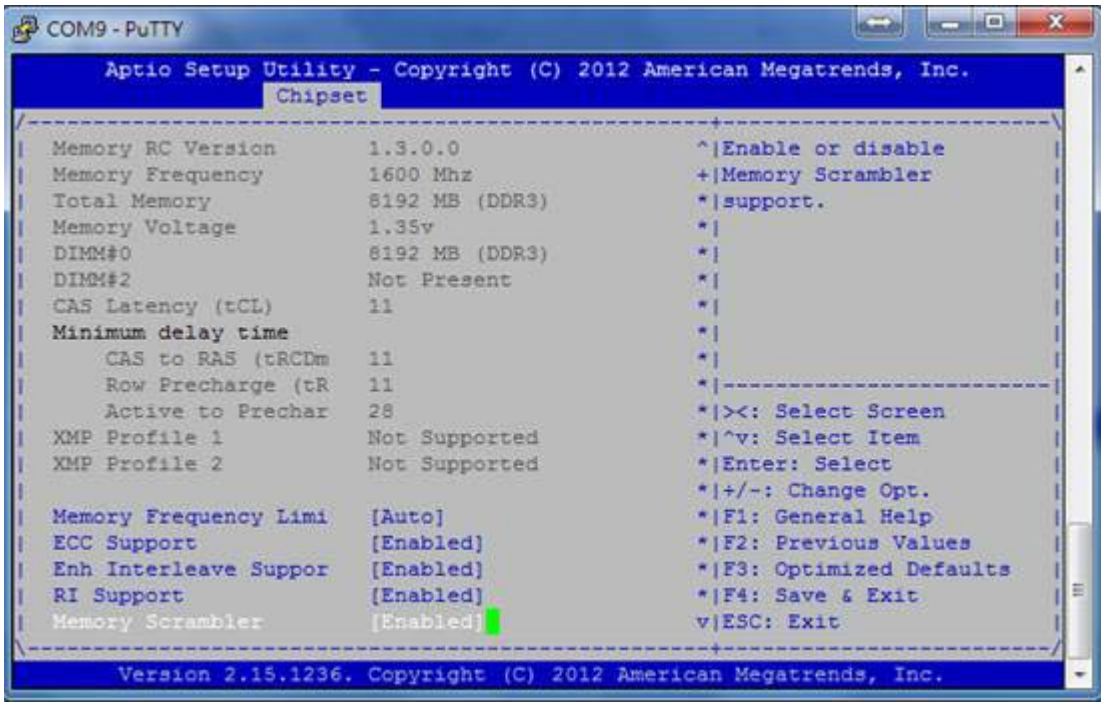


Figure 2.27 Memory Configuration

2.3.3.2 South Bridge Configuration

- **PCI Express Configuration Settings**

  Allow enable or disable PCI Express Root Port

Figure 2.28 PCI Express Configuration

USB Configuration

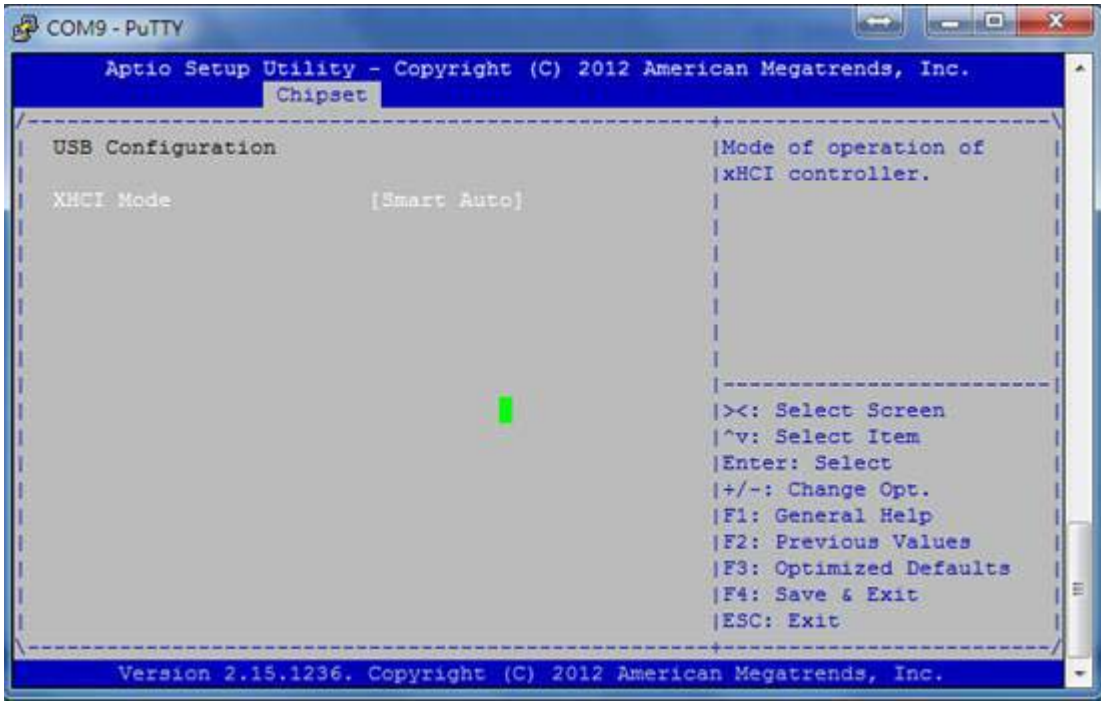


Figure 2.29 USB Configuration

Mode of operation of xHCI controller allows user to enable or disable USB port.

PCH Azalia Configuration

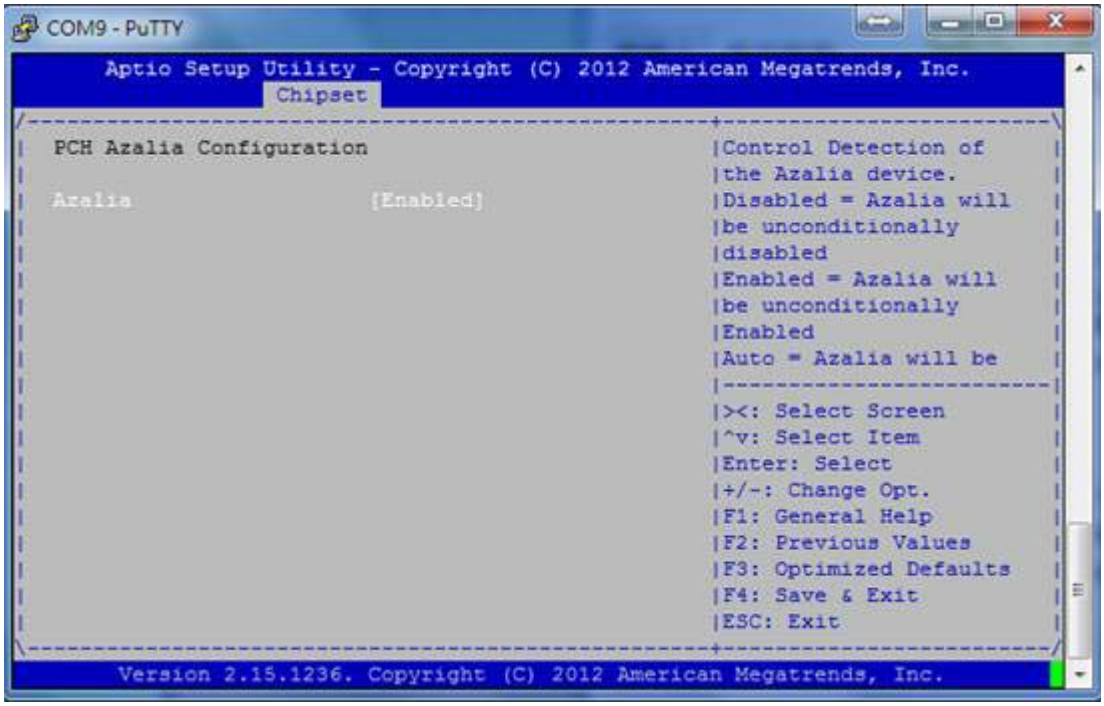


Figure 2.30 PCH Azalia Configuration

Control Detection of the Azalia device.

2.3.4 Boot Configuration

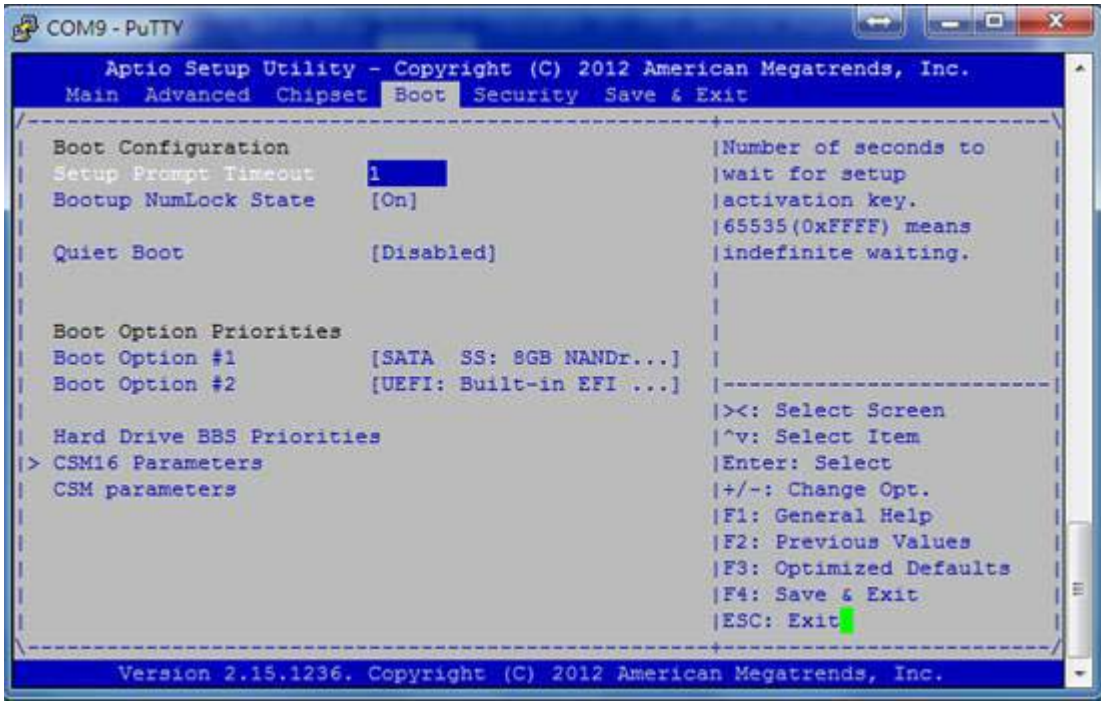


Figure 2.31 Boot Configuration

- **Quiet Boot**
  If this option is set to Disabled, the BIOS display normal POST messages. If enabled, an OEM Logo is shown instead of POST messages.
- **Bootup NumLock State**
  By "ON", the keyboard NumLock state will stay "ON" after booting. By "OFF", the keyboard NumLock state will stay "OFF" after booting.
- **Boot Option Priority**
  Boot Option #1
  Boot Option #2
  Show the boot device choices.
- **Hard Drive BBS Priorities**
  Select the main hard disk device type to be a boot hard drive.

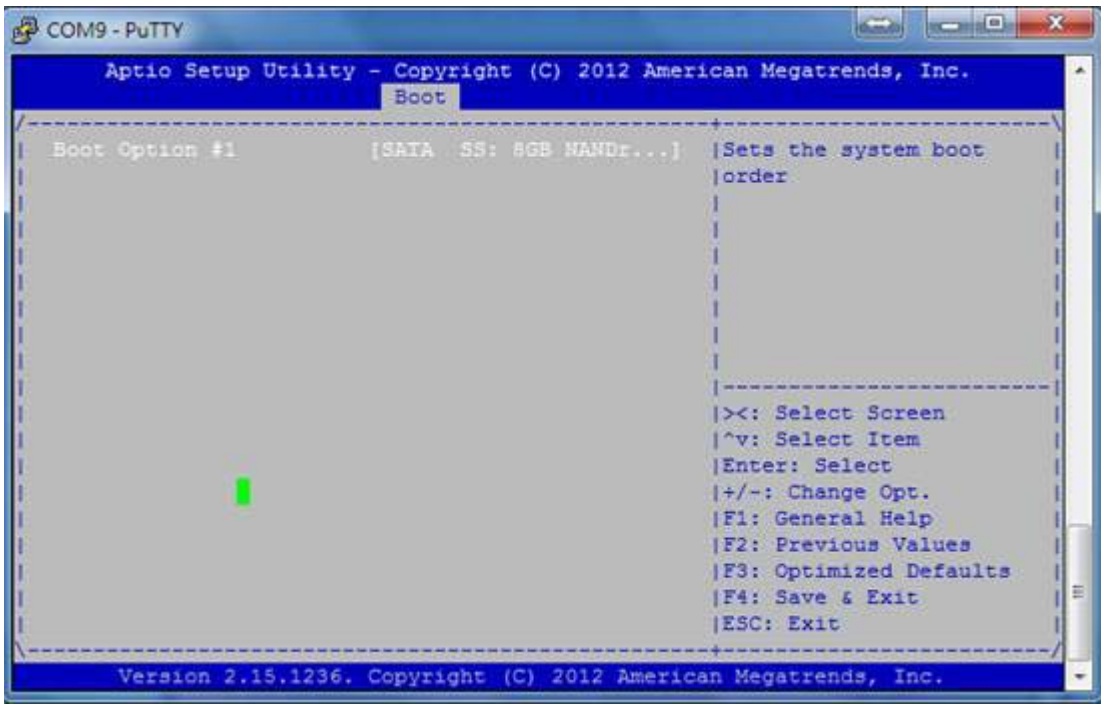


Figure 2.32 Hard Drive BBS Priorities

- **CSM16 Parameters**

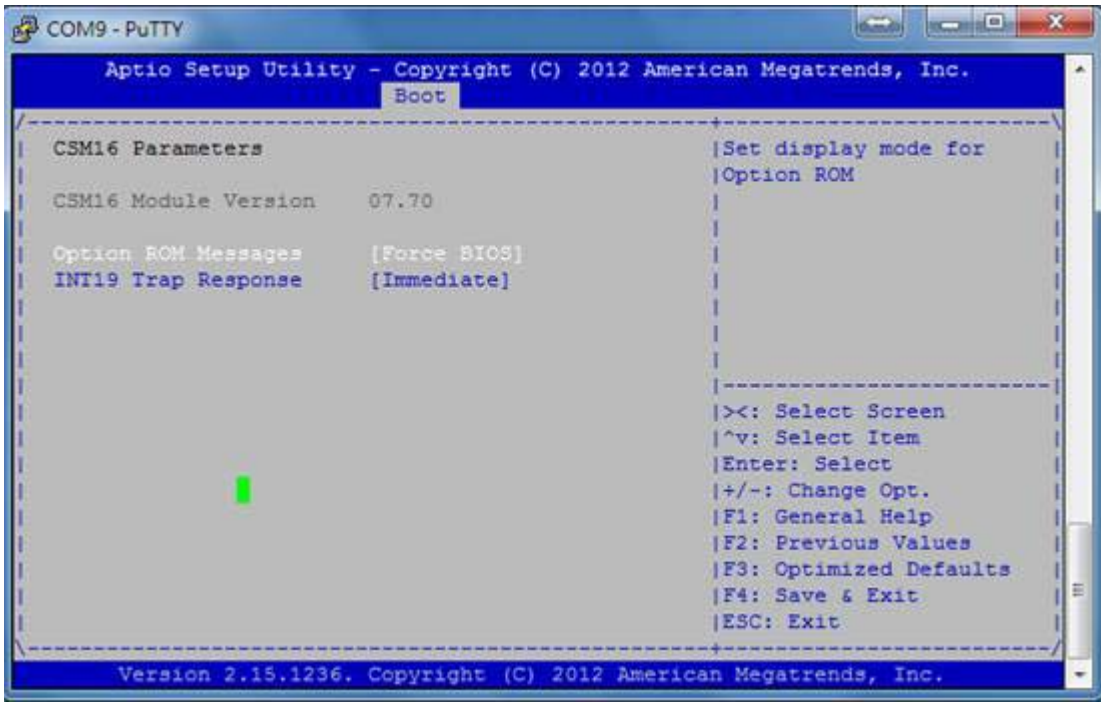


Figure 2.33 CSM16 Parameters

This item allows users to set display mode for Option ROM.

- **CSM Parameters**

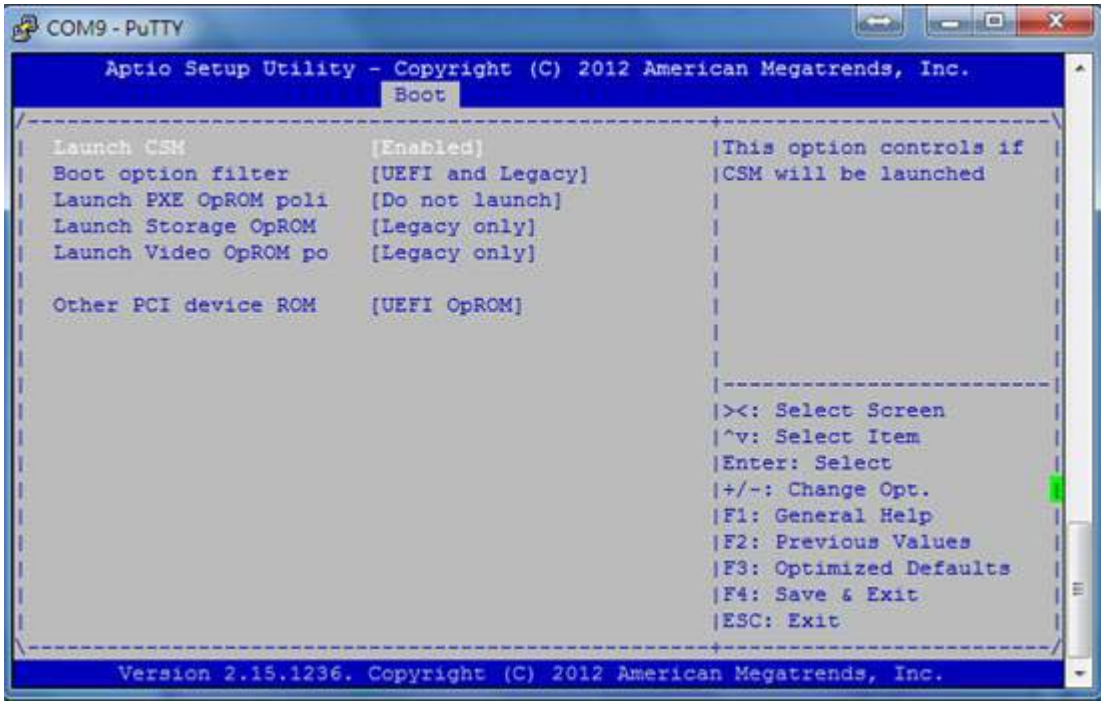


Figure 2.34 CSM Parameters

This option controls if CSM will be launched.

2.3.5 PXE Boot Setting

Enter into Boot setting and choose CSM parameters.

- **Launch PXE OpROM policy**

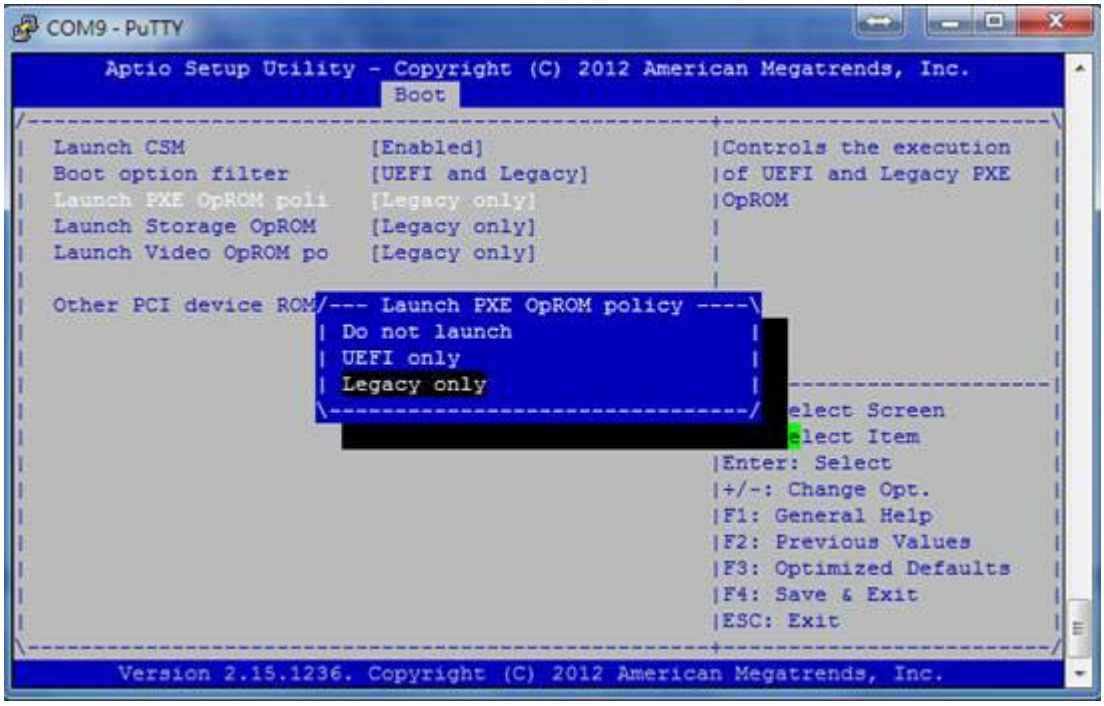


Figure 2.35 Launch PXE OpROM policy

Choose "Legacy only" or "UEFI only" for launch PXE OpROM policy.

- **Save and Exit**

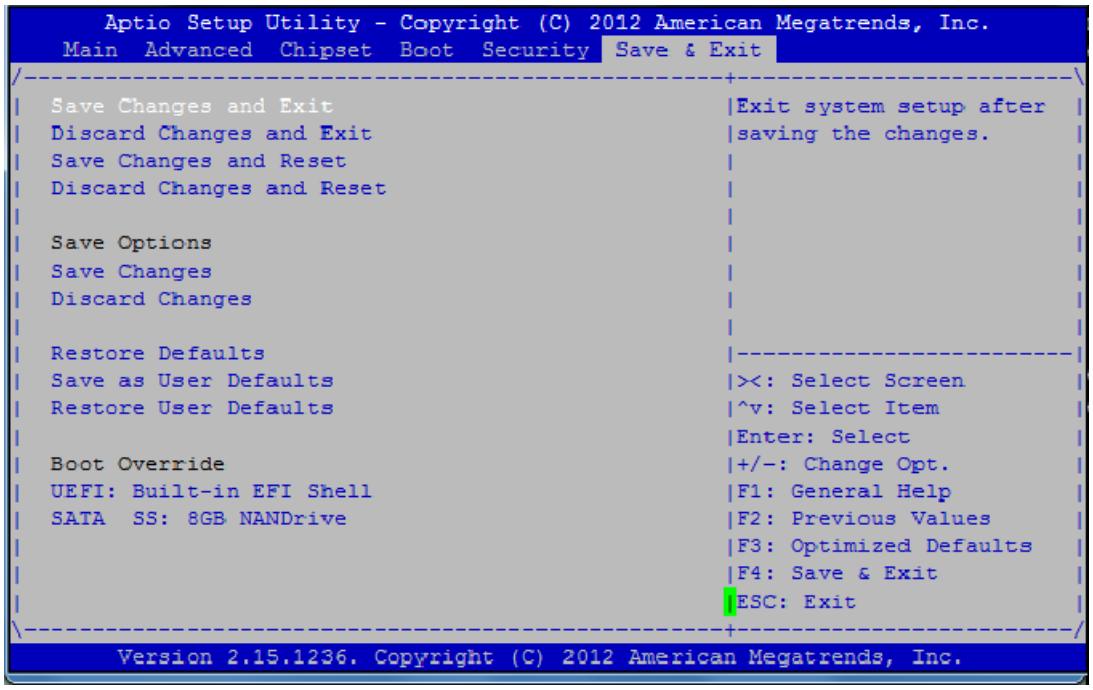
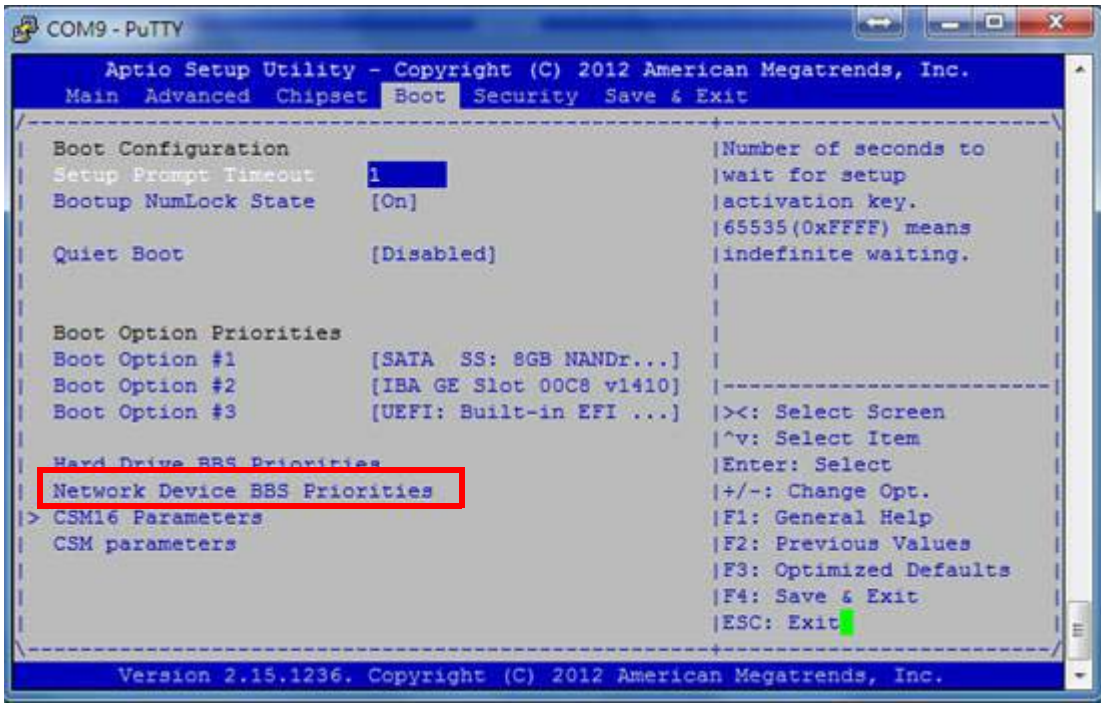
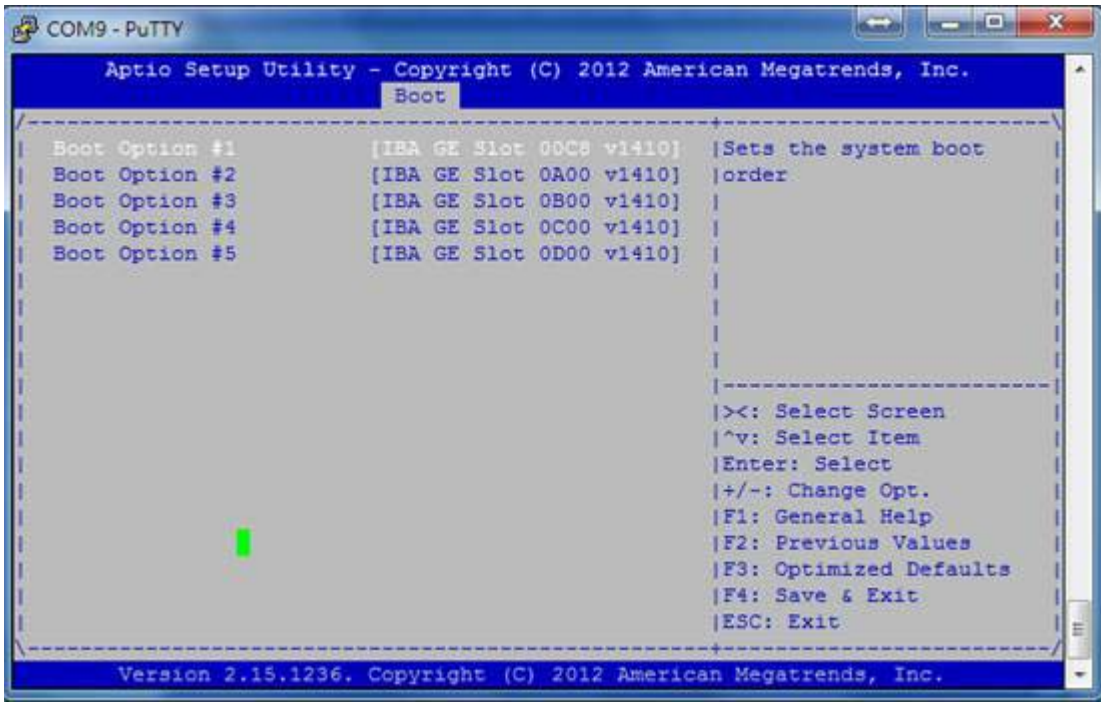


Figure 2.36 Save and Exit

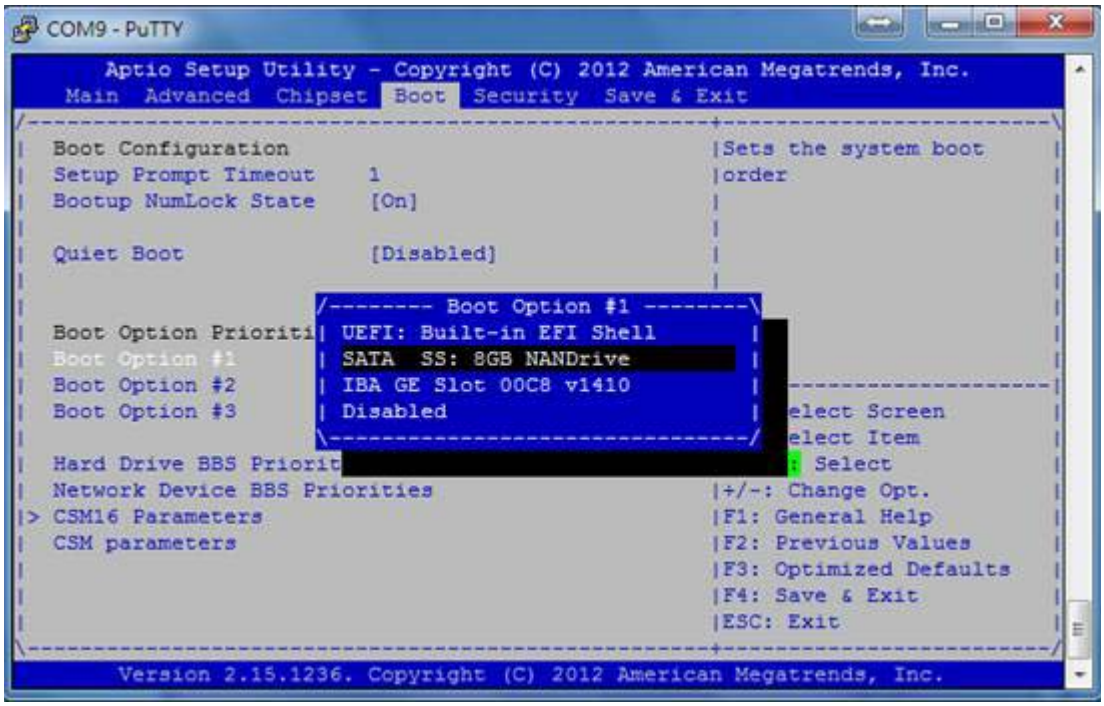
- **Choose boot option priority**

  The "Network device BBS Priorities" will be shown after enabled PXE OpROM.





Note 1: Network Device BBS Priorities



Note 2: Hard Drive BBS Priorities

Figure 2.37 Boot option priority

- **Save Changes and Reset again**

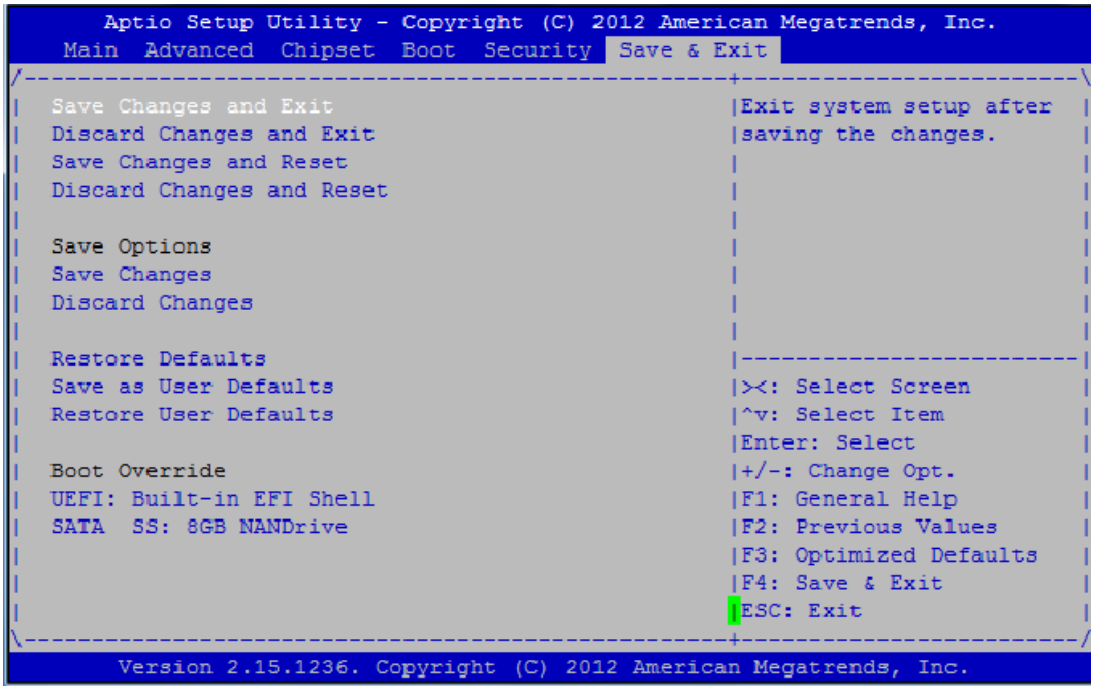


Figure 2.38 Save changes and reset

- **Start PXE Server**

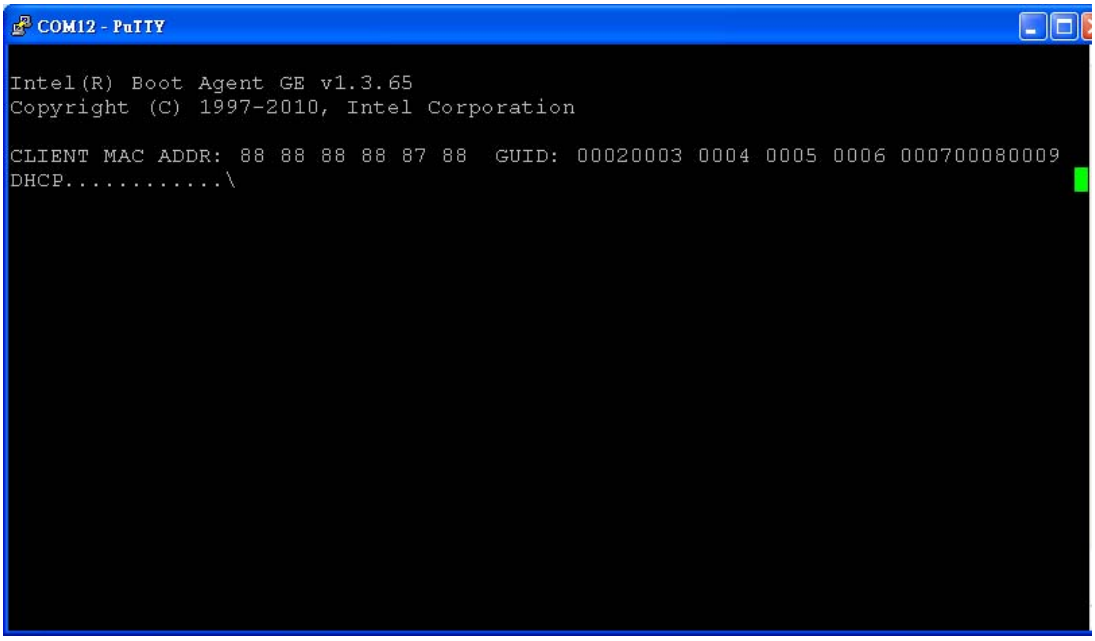


Figure 2.39 Start page of PXE Server

2.3.6 Security Setting

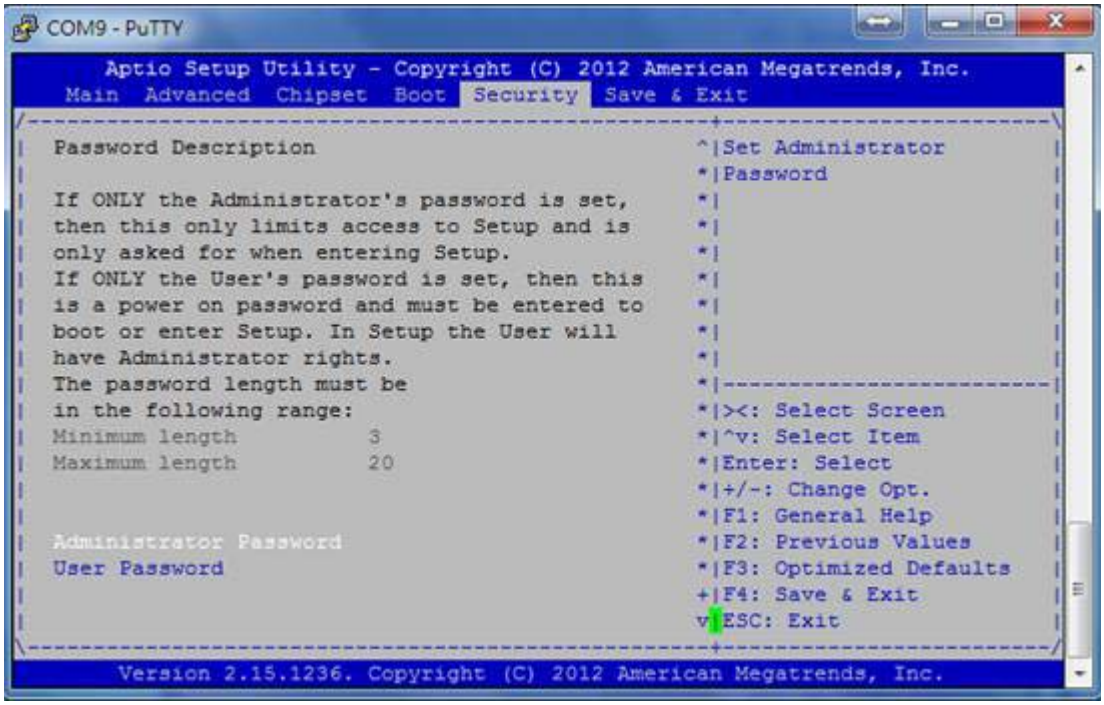


Figure 2.40 Security Setting

- **Administrator Password**
  Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the Administrator password.
- **User Password**
  Select this option and press <ENTER> to access the sub menu, and then type in the password. Set the User Password.

2.3.7 Save & Exit Option

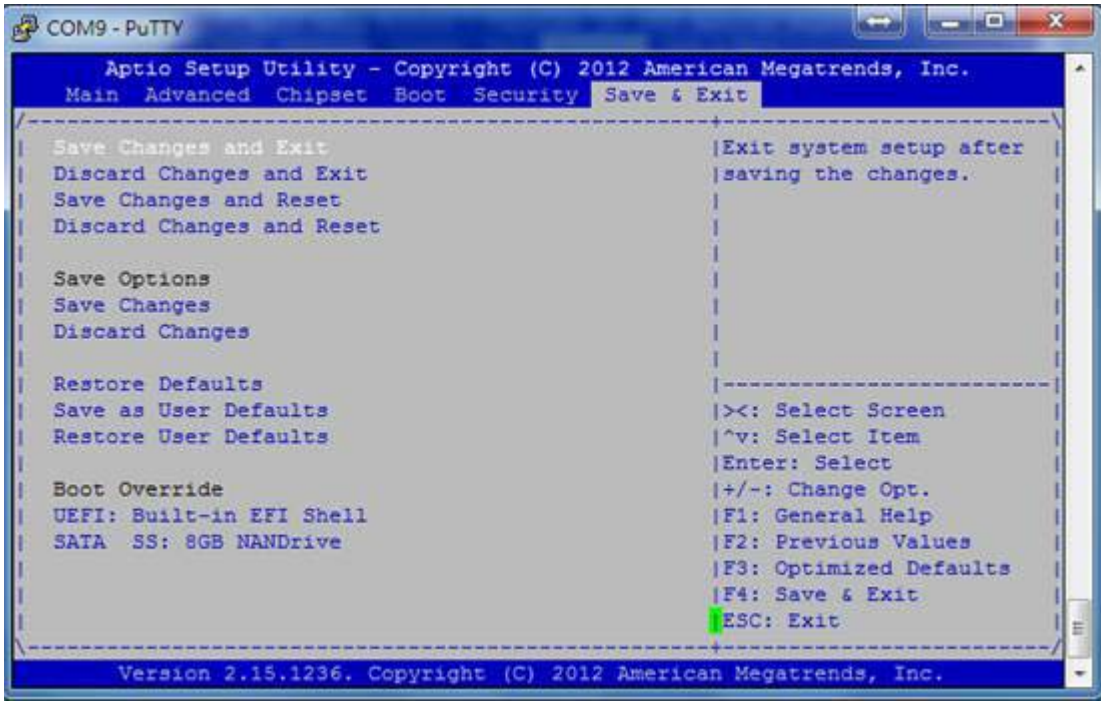


Figure 2.41 Save and Exit

- **Save Changes and Exit**

  When users have completed system configuration, select this option to save changes, exit BIOS setup menu and reboot the computer to take effect all system configuration parameters.

  1. Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
  2. Select Ok or cancel.

- **Discard Changes and Exit**

  Select this option to quit Setup without making any permanent changes to the system configuration.

  1. Select Exit Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
  2. Select Ok to discard changes and exit. Discard Changes: Select Discard Changes from the Exit menu and press <Enter>.

- **Restore Default**

  The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Defaults if the user's computer is experiencing system configuration problems. Select Restore Defaults from the Exit menu and press <Enter>.

- **Save as User Default**

  Save the all current settings as a user default.

- **Restore User Default**

  Restore all settings to user default values.

- **Boot Override**

  Show the boot device types on the system.

Chapter 3

IPMI for the MIC-3396

This chapter describes IPMI configuration for the MIC-3396.

3.1 Introduction

The MIC-3396 fully supports the major IPMI 2.0 interface and the PICMG 2.9 R1.0 specification. The BMC solution is based on the Advantech IPMI Core G02 and it is designed around a combination of a NXP LPC1768 ARM Cortex-M3 based 32 bit microcontroller and a Lattice MachXO2 series FPGA.

The microcontroller is running FreeRTOS as basic OS, with Advantech's own hardware abstraction layer (HAL) and IPMI stack.

The BMC's key features and functions are listed below.

Advantech Integrity Sensor

Based on Advantech IPMI Core, designed for CPCI

- IPMI 2.0 Specification compliant
- IPMI-over-LAN
- Serial-over-LAN
- KCS interface for direct IPMI communication between Operating System and BMC
- Full BMC watchdog support as defines in IPMI specification
- System Event Log (SEL)
- HPM.1 for in field updates, supporting:
  - Bootloader
  - Firmware
  - FPGA
  - BIOS
- Automatic UART muxing between all serial interfaces for easy console access
- Additional sensors for hardware monitoring

3.2 Terms and Definitions

Term	Definition
AMC	Advanced Mezzanine Card
API	Application Programming Interface
ATCA	Advanced Telecommunications Computing Architecture
BIOS	Basic Input/Output System
BMC	Baseboard Management Controller
CLI	Command Line Interface
CPCI	CompactPCI
CPU	Central Processing Unit
DDR3	Double Data Rate 3
DIMM	Dual In-line Memory Module
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
FLASH	Flash memory
FPGA	Field Programmable Gate Array
FRU	Field Replaceable Unit
GbE	Gigabit Ethernet
GPIO	General Purpose Input / Output
HPM.1	Hardware Platform Management.1

I^2C	Inter Integrated Circuit
IPMB	Intelligent Platform Management Bus
BMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
LPC	Low Pin Count (Bus)
NCSI	Network Controller Sideband Interface
NIC	Network Interface Controller
PLD	Programmable Logic Device
RMCP	Remote Management Communication Protocol
RS232	Recommended Standard 232
SAS	Serial Attached Storage
SATA	Serial Advanced Technology Attachment
SDR	Sensor Data Record
Sensor Data Repository	
SEL	System Event Log
SPI	Serial Peripheral Interface
UART	Universal Asynchronus Receiver Transmitter
USB	Universal Serial Bus
XMC	XMC mezzanine card (Vita 42.0)

3.3 IPMI Interfaces

The MIC-3396 provides three main IPMI messaging interfaces to connect to the BMC. There are the IPMB-0 for main messaging interface between CPCI boards, the LAN side band interface (NCSI) and the on-board payload interface to x86 (KCS).

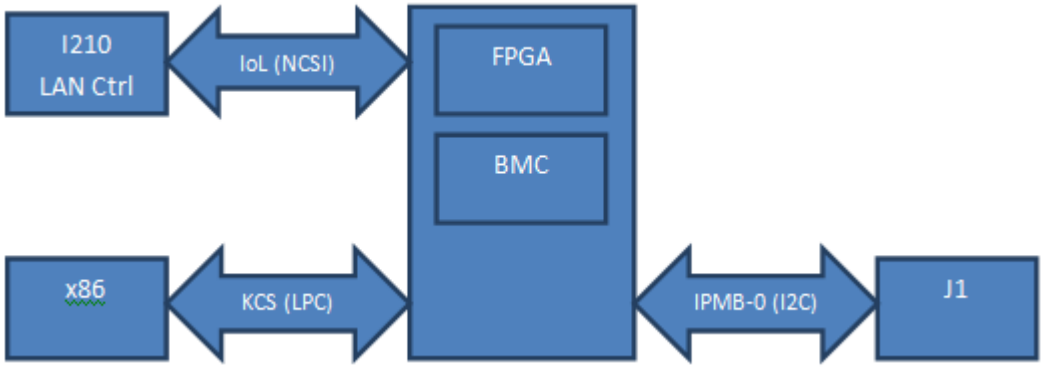


Figure 3.1 Management part block diagram

3.3.1 IPMB-0

IPMB-0 is the I^2C-based PICMG 2.9 R1.0 defined main messaging interface between CPCI boards. It consists of one I^2C bus clocked at a frequency of 100 kHz, using IPMI compliant messaging.

3.3.2 KCS

The BMC's KCS interface is implemented according to the IPMI 2.0 specification.

Keyboard Controller Style (KCS) interfacing describes a legacy system interface based around a bidirectional set of a status/command and data register.

This kind of interface has been adopted as system interface in IPMI and provides the benefits of:

- Higher bandwidth than I^2C or RS232 based interfaces.
- Robustness.
- Auto-discovery options

3.3.3 LAN

The BMC FW supports a LAN interface providing NSCI according to the IPMI 2.0 specification

The BMC is attached to an Intel I210 network controller (LAN2) that is supporting a sideband interface (NC-SI).

The table below lists the supported network protocols.

Table 3.1: Supported Network Protocols

Mnemonic	Protocol
ARP	Address Resolution Protocol
ICMP	Internet Control Message Protocol
IP	Internet Protocol
UDP	User Datagram Protocol
RMCP/RMCP+	Remote Management Control Protocol

3.3.3.1 ARP

Both standard ARP requests and reply (ARP opcodes 0x01 and 0x02) are supported to propagate the BMC's IP address in the system. Gratious ARP is supported for dynamic address changes or failover scenarios. Other ARP opcodes are not supported and will be ignored.

3.3.3.2 ICMP

ICMP is supported to allow network pings to/from the BMC.

3.3.3.3 RMCP/RMCP+

IPMI over LAN (IOL) uses RMCP as messaging protocol as defined in the IPMI specifications. RMCP messages consist of the basic IPMI message with some RMCP specific overhead and use the UDP protocol for data transmission.

UDP in turn uses the IP protocol for data transport, so the network stack needs to support the IP and UDP protocols along with RMCP.

RMCP+ was added in the IPMI v2.0 specification. It's an enhanced protocol for transferring IPMI messages and other types of payloads (e.g. serial data).

3.4 Command Line Interface

The Advantech IPMI core supports besides the IPMI defined interfaces a command line interface to grant easy and fast human readable system information. This can be used for debugging and error recovery as well as showing information about the board and firmware status. The command line interface (CLI) is implemented on UART 0 and accepts high level commands as well as IPMI messages in “Serial Terminal Mode” as specified in IPMI 1.5.

The CLI uses a baud rate of 115200, 8 data bits, 1 stop bit and no parity.

Table 3.2: Standard CLI Commands

Command	Description
[…]	Any value between this brackets will be interpreted as IPMI message
<Enter>	Confirm Input
<Up>	Step through history
bios_hist	Show BIOS POST code history
debug	Switch to serial debug console ('q' or 'x' to exit)
help	Print command overview
info	Print FW and product information
memory_pres	Show memory DIMM presence status
ncsi_status	Print detailed NC-SI status
ncsi_table	Print NC-SI link status table
reboot	Reboot
spidump	Dump all FPGA SPI registers
switch_debug	Switch On/Off messaging interfaces in Debug output

3.5 BMC Watchdog

The BMC provides an IPMI 2.0 compliant BMC Watchdog to monitor the OS during runtime or to observe the BIOS boot progress.

3.5.1 BIOS Boot Watchdog

The IPMI compliant BMC Watchdog is used to monitor BIOS boot progress and initiate a rollback when a BIOS is found to be corrupt.

It is set to a predefined value of 180 seconds and automatically starts when the payload power for the x86 subsystem is being turned on. The time out action is set to “hardware reset”, with the timer use indicating BIOS use.

If the watchdog timer times out with this configuration, it triggers a BIOS chip failover followed by a system reset and restart of the watchdog timer. The mechanism runs in an endless loop and logs timeouts + failovers to the SEL through the Integrity Sensor.

BIOS does not touch the watchdog timer except for two situations:

1. It disables the watchdog right before jumping into the boot loader so it doesn’t trigger after BIOS execution. It could alternatively reconfigure the watchdog to act as boot watchdog (i.e. change timeout action).
2. It temporarily disables the watchdog once the setup menu is manually activated, for debugging purposes.

3.6 System Event Log (SEL)

A 64 kB System Event Log (SEL) is implemented in the BMC. It stores all events that are either generated by the BMC or that are passed to it from the system interface. The events are physically stored in the external attached SPI flash.

All received events are passed to the default event receiver (which typically is the CMM in PICMG2.9 environments if one is present), regardless of being stored in the SEL. This means that local events will show up in the local BMC's SEL as well as in the CMMs shelf wide SEL, unless there is no filter enabled on the CMM side.

The size of 64 kB is sufficient to hold exactly 4096 entries of 16 bytes each.

Once the SEL is full, it will not store new entries so that existing data is not overwritten. The SBC or System managers can query the SEL usage at any time and it is their responsibility to issue a "SEL Clear" from time to time to avoid local SEL overflow.

3.7 Sensors

All important voltages and temperatures are connected to the BMC management system in different ways.

Moreover, the BMC also registers some logical sensors listed below:

- BMC Watchdog sensor
- FW Progress sensor
- Version change sensor
- Advantech OEM Sensor: Integrity Sensor

3.7.1 Sensor List

The following table specifies all sensors provided by the BMC:

Table 3.3: BMC sensor list

No.	Sensor ID	Sensor Type (Event/Reading Type)	Description
0	BMC_WATCHDOG	Watchdog 2 (Discrete)	IPMI BMC Watchdog sensor
1	FW_PROGRESS	System Firmware Progress (Discrete)	IPMI FW Progress sensor
2	VERSION_CHANGE	Version Change (Discrete)	IPMI Version Change sensor
3	PROC_VR_HOT	OEM (Discrete)	Processor HOT status and Voltage regulator HOT Status
4	THERM_TRIP	OEM (Discrete)	CPU Thermal Trip
5	BAT_3_0-VOL	Voltage (Threshold)	Battery voltage
6	SB_3_3-VOL	Voltage (Threshold)	Standby Power voltage 3.3V
7	SB_5_0_VOL	Voltage (Threshold)	Standby Power voltage 5V
8	PAY_3_3-VOL	Voltage (Threshold)	Payload Power voltage 3.3V
9	PAY_5_0-VOL	Voltage (Threshold)	Payload Power voltage 5V
10	PAY_12-VOL	Voltage (Threshold)	Payload Power voltage 12V
11	PCH_1_05-VOL	Voltage (Threshold)	PCH supply voltage
12	PCH_1_5-VOL	Voltage (Threshold)	PCH supply voltage
13	PCH_1_0-VOL	Voltage (Threshold)	PCH supply voltage
14	CPU_CORE-VOL	Voltage (Threshold)	CPU Core voltage
15	AUX_3_3-VOL	Voltage (Threshold)	Auxiliary voltage 3.3V

Table 3.3: BMC sensor list			
16	HP_3_3-VOL	Voltage (Threshold)	3.3V on the CPCI Connector
17	HP_12_0-VOL	Voltage (Threshold)	12V.0 on the CPCI Connector
18	HP_5_0-VOL	Voltage (Threshold)	5.0V on the CPCI Connector
19	CPU-TMP	Temperature (Threshold)	CPU temperature (PECI)
20	INTEGRITY	OEM	OEM Integrity sensor

3.7.2 Threshold based sensors

Sensor event thresholds are classifies as Non-critical (NC), Critical (CR), or Non-recoverable (NR). This classification is possible in both directions (lower and upper). When different thresholds are reached, different actions may be executed by shelf manager accordingly.

Table 3.4: Sensor Threshold description	
Threshold	**Description**
UNR	Upper Non-Recoverable
UCR	Upper Critical
UNC	Upper Non-Critical
LNC	Lower Non-Critical
LCR	Lower Critical
LNR	Lower Non-Recoverable

3.7.3 Voltage Sensors

The management power voltages and all other payload power voltages are monitored by the BMC.

Table 3.5: Voltage Sensor List							
Sensor Name	**Nominal**	**LNR**	**LCR**	**LNC**	**UNC**	**UCR**	**UNR**
BAT_3_0-VOL	3.00	2.15	2.40	2.60	3.45	3.60	3.70
SB_3_3-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70
SB_5_0_VOL	5.00	4.40	4.50	4.75	5.25	5.50	5.60
PAY_3_3-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70
PAY_5_0-VOL	5.00	4.40	4.50	4.75	5.25	5.50	5.60
PAY_12-VOL	12.0	9.90	10.2	10.8	13.2	13.8	14.1
PCH_1_05-VOL	1.05	0.88	0.945	0.99	1.11	1.155	1.22
PCH_1_5-VOL	1.5	1.26	1.35	1.425	1.575	1.65	1.74
PCH_1_0-VOL	1.00	0.88	0.90	0.93	1.07	1.10	1.12
CPU_CORE-VOL	1.80	1.58	1.62	1.71	1.89	1.98	2.02
AUX_3_3-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70
HP_3_3-VOL	3.30	2.90	3.00	3.15	3.45	3.60	3.70
HP_5_0-VOL	5.00	4.40	4.50	4.75	5.25	5.50	5.60
HP_12_0-VOL	12.0	9.90	10.2	10.8	13.2	13.8	14.1

3.7.4 Temperature Sensors

Several temperature sensors are supported, either via board populated IC's or Intel PECI readings from CPU.

Table 3.6: Temperature Sensor List

Sensor Name	Nominal	LNR	LCR	LNC	UNC	UCR	UNR
CPU-TMP	40	-15	-10	-5	80	90	105

3.7.5 Integrity Sensor

The Integrity Sensor is an OEM sensor according to the SDR (Sensor Data Record) definitions in the IPMI specification. It is used to observe the system while operating. In case of the occurrence of predefined conditions or actions, it throws events. Consequently there are generated entries in the System Event Log. So the user is able to trace back detailed possible errors or executed actions of the firmware.

The event message contains three bytes of event data. Byte 1 is the IPMI header, which is a fixed value 0xA0. Byte 2 satisfies the logical component, while byte 3 stands for its action. The table below shows the supported event code structure generated by the integrity sensors on the MIC-3396.

Table 3.7: Integrity Sensor event data table

Component	Action / Subcomponent	Result	Byte 1	Byte 2	Byte3
BMC FW	Update	Successful	0xA0	0x01	0x00
	Update	Timeout	0xA0	0x01	0x04
	Update	Aborted	0xA0	0x01	0x02
	Activation	Failed	0xA0	0x01	0x21
	Manual Rollback	Initiated	0xA0	0x01	0x15
	Automatic Rollback	Initiated	0xA0	0x01	0x1D
	Rollback	Finished	0xA0	0x01	0x0E
	Rollback	Failed	0xA0	0x01	0x09
	Graceful Shutdown	Timeout	0xA0	0x01	0x74
FPGA	Update	Successful	0xA0	0x02	0x00
	Update	Timeout	0xA0	0x02	0x04
	Update	Aborted	0xA0	0x02	0x02
	Recovery	Finished	0xA0	0x02	0x0E
BIOS	Update	Successful	0xA0	0x03	0x00
	Update	Timeout	0xA0	0x03	0x04
	Update	Aborted	0xA0	0x03	0x02
	Flash 0 Boot	Failed	0xA0	0x03	0x29
	Flash 1 Boot	Failed	0xA0	0x03	0x31

3.8 OEM IPMI Commands

To provide custom, board-specific functionality, the BMC supports additional commands that are not covered by the PICMG or IPMI specification

Advantech management solutions support extended OEM IPMI command sets, based on the IPMI defined OEM/Group Network Function (NetFn) Codes 2Eh, 2Fh.

The first three data bytes of IPMI requests and responses under the OEM/Group Network Function explicitly identify the OEM vendor that specifies the command functionality. To be more precise, the vendor IANA Enterprise Number for the defining body occupies the first three data bytes in a request, and the first three data bytes following the completion code position in a response.

Advantech's IANA Enterprise Number used for OEM commands is 002839h.

The BMC supports all Advantech IPMI OEM commands listed in below table.

Table 3.8: OEM command list

Command	NetFn	CMD
Store Configuration Settings	2Eh	40h
Read Configuration Settings	2Eh	41h
Read Port 80 (BIOS POST Code)	2Eh	80h
Reload NVRAM defaults	2Eh	81h
Read MAC Address	2Eh	E2h
Load Default Configuration	2Eh	F2h

3.8.1 Store Configuration Command

This command is used to set Product specific settings. The first two bytes (Setting/ Port) are used to select the item that should be changed; the last byte contains the new setting value.

Table 3.9: Store Configuration Settings Command

	byte	data field
Request Data	1:3	Advantech IANA ID (392800h)
	4	Setting 00h - 02h = reserved 03h = Bios 04h = Lan controller 05h = Failure retries 06h = Misc 07h = RTC 08h = FPGA 09h = USB 0Ah = Clock Ekeying 0Bh = PCIe 0Ch = BMC CLI 0Dh = IRQ 0Eh = Carrier Manager
	5	Setting: Bios 00h = Switch Bios Flash Setting: Lan controller Reserved Setting: Failure Retries 00h = Power failure retries 01h = UNR Temperature retries Setting: Misc Reserved Setting: RTC Reserved Setting: FPGA 00h = COM1 UART multiplexer 01h = COM2 UART multiplexer 02h = BMC UART multiplexer Setting: USB Reserved Setting: Clock Ekeying Reserved Setting: PCIe Reserved Setting: CLI 00h = BMC UART Baudrate Setting: IRQ 00h = PROC hot IRQ enabled Setting: Carrier Manager Reserved

Table 3.9: Store Configuration Settings Command

	byte	data field
	6	Setting value that is written to the selected Setting/Port Bytes Bios: Switch Bios Flash 00h = Switch Bios Flashes Lan controller: Lan interface selection Reserved Failure Retries: Power failure retries 00h - FEh = number of failure retries FFh = infinite retries Failure Retries: UNR Temperature retries 00h - FEh = number of failure retries FFh = infinite retries RTC: synchronization Reserved FPGA: COM1 UART multiplexer 00h = not connected 01h = Serial-over-LAN 02h = Frontpanel RJ45 03h = RTM 1 04h = RTM 2 0Bh = BMC_MUX FPGA: COM2 UART multiplexer 00h = not connected 01h = Serial-over-LAN 02h = Frontpanel RJ45 03h = RTM 1 04h = RTM 2 0Bh = BMC FPGA: BMC UART multiplexer 00h = not connected 01h = Frontpanel RJ45 02h = RTM 1 03h = RTM 2 0Bh = SIO1 or 2 CLI: BMC UART Baudrate 00h = 9600 01h = 14400 02h = 19200 03h = 38400 04h = 57600 05h = 115200 IRQ: PROC hot IRQ enabled 00h = disabled 01h = enabled
Response Data	1	Completion Code C7h = request data length invalid C9h = parameter out of range CBh = requested data not present D5h = not supported in present state
	2:4	Advantech IANA ID (392800h)
	5	Setting

3.8.2 Read Configuration Command

This command is used to read Product specific settings. The first two bytes (Setting/ Port) are used to select the item that should be read out, the answer contains the setting value.

Table 3.10: Read Configuration Settings Command

	byte	data field
Request Data	1:3	Advantech IANA ID (392800h)
	4	Setting 00h – 02h = reserved 03h = Bios 04h = Lan controller 05h = Failure retries 06h = Misc 07h = RTC 08h = FPGA 09h = USB 0Bh = PCIe 0Ch = BMC CLI 0Dh = IRQ
	5	5 Port Setting: Bios 00h = Active Bios Flash Setting: Failure Retries 00h = Power failure retries 01h = UNR Temperature retries Setting: FPGA 00h = COM1 UART multiplexer 01h = COM2 UART multiplexer 02h = BMC UART multiplexer Setting: USB Reserved Setting: Clock Ekeying Reserved Setting: PCIe Reserved Setting: CLI 00h = BMC UART Baudrate Setting: IRQ 00h = PROC hot IRQ enabled
Response Data	1	Completion Code C7h = request data length invalid C9h = parameter out of range CBh = requested data not present D5h = not supported in present state
	2:4	Advantech IANA ID (392800h)
	5	Setting

Table 3.10: Read Configuration Settings Command

byte	data field
6	Setting/Port Bytes Bios: Switch Bios Flash 00h = Active BIOS flash Failure Retries: Power failure retries 00h - FEh = number of failure retries FFh = infinite retries Failure Retries: UNR Temperature retries 00h - FEh = number of failure retries FFh = infinite retries Misc: Power budgeting 00h = Dynamic Power Budgeting disabled 01h = Dynamic Power Budgeting enabled FPGA: COM1 UART multiplexer 00h = not connected 01h = Serial-over-LAN 02h = Frontpanel RJ45 03h = Frontpanel miniUSB 04h = RTM 1 05h = RTM 2 FFh = automatic mode FPGA: COM2 UART multiplexer 00h = not connected 01h = Frontpanel RJ45 02h = Frontpanel miniUSB 03h = RTM 1 04h = RTM 2 FPGA: BMC UART multiplexer 00h = not connected 01h = Frontpanel RJ45 02h = Frontpanel miniUSB 03h = RTM 1 04h = RTM 2 CLI: BMC UART Baudrate 00h = 9600 01h = 14400 02h = 19200 03h = 38400 04h = 57600 05h = 115200 IRQ: PROC hot IRQ enabled 00h = disabled 01h = enabled

3.8.3 Read Port 80 Command

This command is used to read out the actual POST code of the UEFI BIOS.

Table 3.11: Read Port 80 command (BIOS POST code)

	byte	data field
Request Data	1:3	Advantech IANA ID (392800h)
Response Data	1	Completion Code
	2:4	Advantech IANA ID (392800h)
	5	POST code

3.8.4 Read MAC Address Command

This command can be used to get the Product MAC addresses.

Table 3.12: Read MAC Address Command

	byte	data field
Request Data	1:3	Advantech IANA ID (392800h)
	4	MAC address number 00h = LAN1 01h = LAN2 02h = LAN3 03h = LAN4 04h = LAN5 05h = BMC NCSI MAC
Response Data	1	Completion Code D5h = not supported in present state
	2:4	Advantech IANA ID (392800h)
	5	MAC address

3.8.5 Reload BMC Default Configuration Command

This command is reloads the Product specific settings.

Table 3.13: Reload BMC Default Configuration Command

	byte	data field
Request Data	1:3	Advantech IANA ID (392800h)
Response Data	1	Completion Code
	2:4	Advantech IANA ID (392800h)

3.9 HPM.1 Upgrade Support

The PICMG HPM.1 (Hardware Platform Management) specification defines a standard way of updating (BMC) firmware components over IPMI based interfaces. Among the mechanism itself, it defines a common update file format and IPMI based commands for the update procedure. HPM.1 is the de facto standard for firmware updates in PICMG based environments.

Advanced features in HPM.1 address redundancy mechanisms, supporting both automatic and manual rollbacks, to properly support the high availability requirements in platforms like CompactPCI.

The Advantech IPMI Core G02 supports HPM.1 updates over any of its IPMI interfaces. See the following tables for a list of HPM.1 components implemented on the CPCI blade and their respective description.

Table 3.14: Supported HPM.1 components

Component	Number
BMC Firmware	0
BMC Boot loader	1
FPGA	2
BIOS	3

3.9.1 Bootloader update

The bootloader HPM.1 upgrade is written to the LPC1768 flash directly. Means there is no recovery existing for the bootloader image. It is not recommended to upgrade the bootloader in the field.

3.9.2 Firmware upgrade

The firmware upgrade component follows the HPM.1 specification and the upgrade and activation stage can be performed while the payload is running. In case of an update, the BMC is not accessible to any service while activation stage.

3.9.3 FPGA upgrade

The firmware upgrade component follows the HPM.1 specification. The upgrade can be performed while the payload is running. For the activation stage, a payload part reboot and power off is required. The BMC is not accessible to any service while activation stage.

3.9.4 BIOS upgrade

Like the FPGA component, the BIOS component requires a payload reboot or power cycle, in order to perform the activation stage. The component follows the HPM.1 standard.

3.10 Board Information

The BMC provides IPMI defined Field Replaceable Unit (FRU) information about the CPCI board and the connected extension modules. The MIC-3396 FRU data include general board information's such as product name, HW version or serial number. A total of 2 kB non-volatile storage space is reserved for the FRU data. The boards IPMI FRU information can be made accessible via all BMC interfaces and the information can be retrieved at any time.

3.10.1 Board Information

Table 3.15: Board Info Area

Field description	Board information
Format version	0x01
Board area length	(calculated)
Language code	0x19(English)
Manufacturer date/time	(based on manufacturing date)
Board manufacturer type/length	0xC9
Board manufacturer	Advantech
Board product name type/length	0xC8
Board product name	MIC-3396
Board serial number type/length	0xCA
Board serial number	(10 characters, written during manufacturing)
Board part number type/length	0xC8
Board part number	MIC-3396
FRU file ID type/length	
FRU file ID	frudata.xml
Additional custom Mfg. Info fields.	(unused)
C1h (No more info fields)	0xC1
00h (unused space)	0x00 0x00 0x00 0x00 0x00
Board area checksum	(calculated)

3.10.2 Product Information

Table 3.16: Product Info Area

Field description	Product information
Format version	0x01
Product area length	(calculated)
Language code	0x19 (English)
Product Manufacturer type/length	0xC9
Product manufacturer	Advantech
Product name type/length	0xC8
Product name	MIC-3396
Product part/model number type/length	0xC8
Product part/model number	MIC-3396
Product version type/length	0xC5
Product version	(Hardware Version)
Product serial number type/length	0xCA
Product serial number	(10 characters, written during manufacturing)
Assert Tag type/length	0xC0
Assert Tag	(unused)
FRU File ID type/length	0xCB
FRU File ID	frudata.xml
Custom product info area fields	(unused)
C1h (no more info fields)	0xC1
00h (any remaining unused space)	0x00
Product area checksum	(calculated)

Appendix A

Pin Assignments

This appendix describes pin assignments.

A.1 J1 Connector

Table A.1: J1 CompactPCI I/O							
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD(1)	5V	V(I/O)	AD(0)	ACK64#	GND
23	GND	3.3V	AD(4)	AD(3)	5V	AD(2)	GND
22	GND	AD(7)	GND	3.3V	AD(6)	AD(5)	GND
21	GND	3.3V	AD(9)	AD(8)	M66EN	C/BE(0)#	GND
20	GND	AD(12)	GND	V(I/O)	AD(11)	AD(10)	GND
19	GND	3.3V	AD(15)	AD(14)	GND	AD(13)	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE(1)#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12-14	KEY AREA						
11	GND	AD(18)	AD(17)	AD(16)	GND	C/BE(2)#	GND
10	GND	AD(21)	GND	3.3V	AD(20)	AD(19)	GND
9	GND	C/BE(3)#	IDSEL	AD(23)	GND	AD(22)	GND
8	GND	AD(26)	GND	V(I/O)	AD(25)	AD(24)	GND
7	GND	AD(30)	AD(29)	AD(28)	GND	AD(27)	GND
6	GND	REQ0#	PRESENT#	3.3V	CLK0	AD(31)	GND
5	GND	NC	NC	PCI_RST#	GND	GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	− 12V	TRST#	＋ 12V	5V	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Note! *NC: No Connection*

#: Active Low

A.2 J2 Connector

Table A.2: J2 CompactPCI I/O							
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	NC	NC	NC	GND
20	GND	CLK5	NC	NC	GND	NC	GND
19	GND	NC	GND	SMB_SDA	SMB_SCL	SMB_ALERT#	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	PRST#	REQ6#	GNT6#	GND
16	GND	NC	NC	DEG#	GND	NC	GND
15	GND	NC	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD(35)	AD(34)	AD(33)	GND	AD(32)	GND
13	GND	AD(38)	GND	V(I/O)	AD(37)	AD(36)	GND
12	GND	AD(42)	AD(41)	AD(40)	GND	AD(39)	GND
11	GND	AD(45)	GND	V(I/O)	AD(44)	AD(43)	GND
10	GND	AD(49)	AD(48)	AD(47)	GND	AD(46)	GND
9	GND	AD(52)	GND	V(IO)	AD(51)	AD(50)	GND
8	GND	AD(56)	AD(55)	AD(54)	GND	AD(53)	GND
7	GND	AD(59)	GND	V(IO)	AD(58)	AD(57)	GND
6	GND	AD(63)	AD(62)	AD(61)	GND	AD(60)	GND
5	GND	C/BE(5)#	GND/64EN#	V(I/O)	C/BE(4)#	PAR64	GND
4	GND	V(I/O)	NC	C/BE(7)#	GND	C/BE(6)#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Note! *NC: No Connection*

#: Active Low

A.3 J3 Connector

PCIe port only support X8 link

Table A.3: J3 CompactPCI I/O (LAN2/LAN3, 2.16)							
Pin	**F**	**A**	**B**	**C**	**D**	**E**	**Z**
1	GND	PCIE_TX12-	PCIE_TX12+	VCC5	PCIE_RX12-	PCIE_RX12+	GND
2	GND	PCIE_TX8+	PCIE_RX8+	VCC5	PCIE_TX9+	PCIE_RX9+	GND
3	GND	PCIE_TX8-	PCIE_RX8-	VCC5	PCIE_TX9-	PCIE_RX9-	GND
4	GND	PCIE_TX13-	PCIE_TX13+	VCC5	PCIE_RX13-	PCIE_RX13+	GND
5	GND	PCIE_TX10+	PCIE_RX10+	PLTRST#	PCIE_TX11+	PCIE_RX11+	GND
6	GND	PCIE_TX10-	PCIE_RX10-	TAP_TMS	PCIE_TX11-	PCIE_RX11-	GND
7	GND	PCIE_TX14-	PCIE_TX14+	TAP_TCK	PCIE_RX14-	PCIE_RX14+	GND
8	GND	PCIE_CLK+	USB3_6TX+	TAP_TRST#	USB3_2TX+	USB3_2RX+	GND
9	GND	PCIE_CLK-	USB3_6TX-	TAP_TDI	USB3_2TX-	USB3_2RX-	GND
10	GND	PCIE_TX15-	PCIE_TX15+	TAP_TDO	USB3_6RX-	USB3_6RX+	GND
11	GND	GND	GND	VCC3	PCIE_RX15-	PCIE_RX15+	GND
12	GND	SATA4_TX+	SATA4_RX+	VCC3	SATA5_TX+	SATA5_RX+	GND
13	GND	SATA4_TX-	SATA4_RX-	VCC3	SATA5_TX-	SATA5_RX-	GND
14	GND	GND	GND	VCC3	GND	GND	GND
15	GND	MDIB1+	MDIB1-	GND	MDIB3+	MDIB3-	GND
16	GND	MDIB0+	MDIB0-	GND	MDIB2+	MDIB2-	GND
17	GND	MDIA1+	MDIA1-	GND	MDIA3+	MDIA3-	GND
18	GND	MDIA0+	MDIA0-	GND	MDIA2+	MDIA2-	GND
19	GND	NC	NC	SATA_LED#	NC	NC	GND

Note! *NC: No Connection*

#: Active Low

A.4 J4 Connector

Table A.4: J4 CompactPCI I/O port							
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**
1	GND	UART_TXD3	NC	GND	DDI2_AUX+	USB1_VCC	GND
2	GND	UART_RXD3	NC	GND	DDI2_AUX-	USBD1-	GND
3	GND	UART_RTS3	GND	GND	NC	USBD1+	GND
4	GND	NC	NC	GND	DDI2_PAIR0+	GND	GND
5	GND	NC	NC	GND	DDI2_PAIR0-	USB3_VCC	GND
6	GND	NC	NC	GND	DDI2_PAIR1+	USBD3-	GND
7	GND	NC	NC	GND	DDI2_PAIR1-	USBD3+	GND
8	GND	NC	NC	GND	DDI2_PAIR2+	GND	GND
9	GND	NC	NC	GND	DDI2_PAIR2-	DDI2_DDC_CLK	GND
10	GND	NC	NC	GND	DDI2_PAIR3+	DDI2_DDC_DAT	GND
11	GND	NC	NC	GND	DDI2_PAIR3-	DDI2_HPD	GND
12-14							
15	GND	NC	NC	GND	AUDIO_GND	MIC_L	GND
16	GND	NC	NC	GND	NC	MIC_R	GND
17	GND	NC	GND	GND	LINE_JD	LINEIN_L	GND
18	GND	NC	NC	GND	LINEOUT_L	LINEIN_R	GND
19	GND	NC	NC	GND	LINEOUT_R	TBD (LOUT_L)	GND
20	GND	NC	NC	GND	AUDIO_GND	TBD (LOUT_R)	GND
21	GND	NC	NC	GND	DDI2_DVIPWR	AUDIO_GND	GND
22	GND	NC	NC	GND	NC	NC	GND
23	GND	NC	NC	GND	NC	NC	GND
24	GND	J4_GPIO1	NC	GND	NC (VBAT)	NC	GND
25	GND	J4_GPIO2	NC	GND	PRST#	NC	GND

Note! *NC: No Connection*

#: Active Low

A.5 J5 Connector

Table A.5: J5 CompactPCI I/O port							
Pin	**F**	**A**	**B**	**C**	**D**	**E**	**Z**
1	GND	RTM_MDIA0+	RTM_MDIA0-	GND	RTM_MDIA1+	RTM_MDIA1-	GND
2	GND	RTM_MDIA2+	RTM_MDIA2-	GND	RTM_MDIA3+	RTM_MDIA3-	GND
3	GND	RTM_MDIB0+	RTM_MDIB0-	GND	RTM_MDIB1+	RTM_MDIB1-	GND
4	GND	RTM_MDIB2+	RTM_MDIB2-	GND	RTM_MDIB3+	RTM_MDIB3-	GND
5	GND	NC	GND	DDI1_DVIPWR	NC	NC	GND
6	GND	DDI1_AUX+	GND	DDI1_DDC_DAT	USB11_PWR	USB10_PWR	GND
7	GND	DDI1_AUX-	GND	DDI1_DDC_CLK	USBD11+	USBD10+	GND
8	GND	DDI1_PAIR0+	GND	MSDAT	USBD11-	USBD10-	GND
9	GND	DDI1_PAIR0-	GND	MSCLK	GND	GND	GND
10	GND	DDI1_PAIR1+	GND	PS2PWR	USB12_PWR	VGA_DDC_DAT	GND
11	GND	DDI1_PAIR1-	GND	KBDAT	USBD12+	VGA_DDC_CLK	GND
12	GND	DDI1_PAIR2+	GND	KBCLK	USBD12-	VGA_PWR	GND
13	GND	DDI1_PAIR2-	GND	DDI1_HPD	GND	VGA_VSYNC	GND
14	GND	DDI1_PAIR3+	GND	2.16A_LINK1000#	USB13_PWR	VGA_HSYNC	GND
15	GND	DDI1_PAIR3-	GND	2.16A_LIN100#	USBD13+	VGA_RED	GND
16	GND	RTMA_LINK1000#	RTMB_LINK100#	2.16A_LINK-ACT#	USBD13-	VGA_GREEN	GND
17	GND	RTMA_LINK100#	RTMB_LINK1000#	2.16B_LINK100#	GND	VGA_BLUE	GND
18	GND	RTMA_LINK-ACT#	RTMB_LINK-ACT#	2.16B_LINK1000#	UART2_RTS	GND	GND
19	GND	COM1_RX#	COM1_CTS#	2.16B_LINK-ACT#	COM2_DCD#	COM2_TX#	GND
20	GND	COM1_TX#	COM1_DSR#	RTM_PRES#	COM2_RTS#	COM2_DTR#	GND
21	GND	COM1_RTS#	COM1_DTR#	UART2_TXD	COM2_CTS#	COM2_RI#	GND
22	GND	COM1_DCD#	COM1_RI#	UART2_RXD	COM2_DSR#	COM2_RX#	GND

Note! *NC: No Connection*

#: Active Low

A.6 Other Connector

Table A.6: SATA1 Daughter Board Connector			
1	GND	2	GND
3	SATA0_TX+	4	NC
5	SATA0_TX-	6	NC
7	GND	8	GND
9	SATA0_RX+	10	NC
11	SATA0_RX-	12	NC
13	GND	14	GND
15	GND	16	GND
17	VCC5	18	VCC3
19	VCC5	20	VCC3

Table A.7: J15(P15) XMC1 Connector						
Pin	**A**	**B**	**C**	**D**	**E**	**F**
1	PETX_P0	PETX_N0	+3.3V	PETX_P1	PETX_N1	VPWR(+5V)
2	GND	GND	NC(JRST#)	GND	GND	PRST#
3	PETX_P2	PETX_N2	+3.3V	PETX_P3	PETX_N3	VPWR(+5V)
4	GND	GND	NC(JTCK)	GND	GND	NC(MRSTO#)
5	PETX_P4	PETX_N4	+3.3V	PETX_P5	PETX_N5	VPWR(+5V)
6	GND	GND	NC(JTMS)	GND	GND	+12V
7	PETX_P6	PETX_N6	+3.3V	PETX_P7	PETX_N7	VPWR(+5V)
8	GND	GND	NC(JTDI)	GND	GND	-12V
9	NC	NC	NC	NC	NC	VPWR(+5V)
10	GND	GND	NC(JTDO)	GND	GND	GA0
11	PERX_P0	PERX_N0	NC(MBIST#)	PERX_P1	PERX_N1	VPWR(+5V)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PERX_P2	PERX_N2	NC(+3.3V_AUX)	PERX_P3	PERX_N3	VPWR(+5V)
14	GND	GND	GA2	GND	GND	TBD_SDA
15	PERX_P4	PERX_N4	NC	PERX_P5	PERX_N5	VPWR(+5V)
16	GND	GND	NC(MVMRO)	GND	GND	TBD_SCLK
17	PERX_P6	PERX_N6	NC	PERX_P7	PERX_N7	NC
18	GND	GND	FPGAIO1	GND	GND	NC
19	CLK_100Mhz	CLK_100Mhz#	FPGAIO2	NC(WAKE#)	NC(ROOT#)	NC

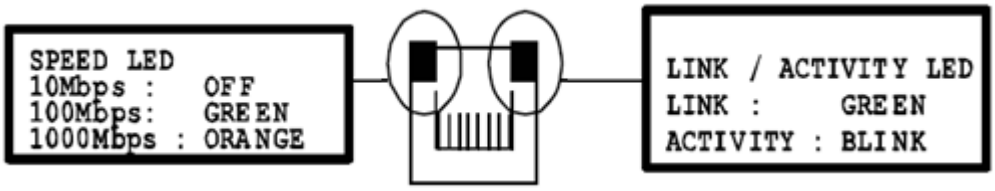
Table A.8: VGA1 Connector			
1	RED	9	+5V
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	DDC_DATA
5	DET#	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDC_CLK
8	GND		

Table A.9: COM1 (RJ45) Connector			
1	DCD#	6	DSR#
2	SIN (RX)	7	RTS#
3	SOUT(TX)	8	CTS#
4	DTR#		
5	GND		

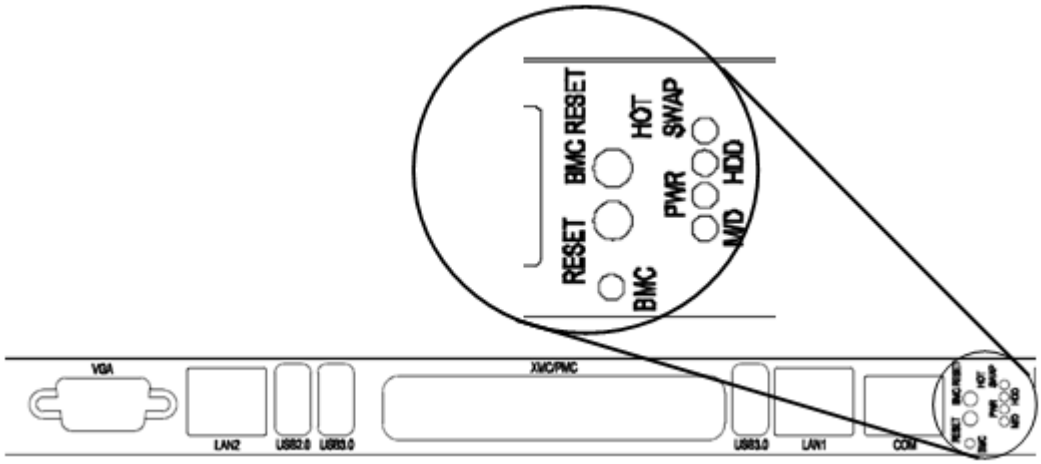
Table A.10: USB2CN1, USB3CN1 & USB3CN2					
USB2CN1		**USB3CN1**		**USB3CN2**	
1	+5V (fused)	1	+5V (fused)	1	+5V (fused)
2	USBD0-	2	USBD1-	2	USBD1-
3	USBD0+	3	USBD1+	3	USBD1+
4	GND	4	GND	4	GND
		5	SSRX-	5	SSRX-
		6	SSRX+	6	SSRX+
		7	GND	7	GND
		8	SSTX-	8	SSTX-
		9	SSTX+	9	SSTX+

Table A.11: BH1 CMOS battery			
1	BAT_VCC	2	GND

Table A.12: RJ45 LAN Connector			
1	LAN_0+	5	LAN_2-
2	LAN_0-	6	LAN_1-
3	LAN_1+	7	LAN_3+
4	LAN_2+	8	LAN_3-



A.6.1 M/D, PWR, BMC, HDD and Hot-swap LEDs



Name	Description
M/D (Green)	Indicates Master or Drone mode status
PWR (Green)	Indicates power status
HDD (Yellow)	Indicates BMC status (heart beat to indicate BMC active)
Hot Swap (Blue)	Indicates the board is ready to be hot-swapped.
BMC (Green)	Indicates BMC status

Appendix B

Programming the Watchdog Timer

This appendix describes how to program the watchdog timer.

Watchdog Timer Programming Procedure

To program the watchdog timer, you must execute a program that writes a value to I/O port address 443/444 (hex) for Enable/Disable. This output value represents time interval. The value range is from 01 (hex) to FF (hex), and the related time interval is 1 to 255 seconds.

Data	Time Interval
01	1 sec
02	2 sec
03	3 sec
04	4 sec
...	
3F	63 sec

After data entry, your program must refresh the watchdog timer by rewriting the I/O port 443 and 443 (hex) while simultaneously setting it. When you want to disable the watchdog timer, your program should read I/O port 444 (hex). The following example shows how you might program the watchdog timer in BASIC:

```
10 REM Watchdog timer example program
20 OUT &H443, data REM Start and restart the watchdog
30 GOSUB 1000 REM Your application task #1,
40 OUT &H443, data REM Reset the timer
50 GOSUB 2000 REM Your application task #2,
60 OUT &H443, data REM Reset the timer
70 X=INP (&H444) REM, Disable the watchdog timer
80 END
1000 REM Subroutine #1, your application task
.
1070 RETURN
2000 REM Subroutine #2, your application task
.
2090 RETURN
```

Appendix C

FPGA

This appendix describes FPGA configuration.

C.1 Overview

Advantech BMC solution combines a NXP LPC1768 ARM Cortex-M3 based 32-bit microcontroller and a Lattice XP2 series FPGA. The FPGA mainly integrates hardware interfaces which are not available or not available in the right amount inside the LPC1768, like I^2C or KCS.

As the MIC-3396 will be available in versions both with and without the BMC, some functions will be implemented redundant inside the FPGA and BMC. If the BMC is populated, a simple register inside the FPGA is used to control the regarding function from the BMC. On a MIC-3396 without BMC the FPGA controls the function by itself in the same way as before.

C.2 Features

- Drone Mode
- Hot-Swap: Hot insertion and removal control
- CompactPCI Backplane: CompactPCI slot Addressing
- LPC Interface: Provides LPC Bus access
- KCS Interface: Standard IPMI payload interface from x86 to BMC
- Watchdog
- Debug Message: Boot time POST message

C.3 FPGA I/O Registers

The Advantech MIC-3396 FPGA communicates with main I/O spaces. The LPC unit is used to interconnect the Intel QM87 LPC signals. The Debug Port Unit is used to decode POST codes. The Hot-Swap Out-Of-Service LED Control Unit is used to control the blue LED during Hot-Insert and Hot-Remove. The Drone Mode Unit is used to disable the CPCI Bridge. The other signals in the Miscellaneous Unit are for interfacing with corresponding I/O interface signals.

Table C.1: LPC I/O registers address

LPC Address	I/O Type	Description
0x 80	W	Port 80 Display
0x440	R	FPGA Minor Version
0x442	R	UART_MUX Switch
0x443 ~ 0x444	RW	Watchdog Register
0x445	R	FPGA Major Version
0x446	R	BIOS Flash Control
0x447	R	Geographical Address (GA)
0x448	R	HW Revision
0x44A	RW	GPIO Control
0x44C	R	FPGA ID
0x44F	RW	Scratch Register
0x4A0 ~ 0x4A7	RW	I2C Interface & Control
0x4B0 ~ 0x4B8	RW	SPI Interface & Control
0xCA2 ~ 0xCA3	RW	KCS Interface

Appendix D

Glossary

ACPI	Advanced Configuration and Power Interface
BMC	Baseboard Management Controller
CF	CompactFlash
CPU	Central Processing Unit
CPCI	CompactPCI
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Checking and Correction
EDMA	Enhanced DMA
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro Magnetic Compatibility
ESD	Electro Static Discharge
FCBGA	Flip Chip BGA
FSB	Front Side Bus
HDD	Hard Disk Drive
HW	HardWare
I/O	Input/Output
IC	Integrated Circuit
IMCH	Integrated Memory Controller Hub
LED	Light Emitting Diode
LPC	Low Pin Count
LV	Low Voltage
MAC	Medium Access Control
OS	Operating System
PCB	Printed Wiring Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PHY	Physical layer Interface
RASUM	Reliability, Availability, Serviceability, Usability and Manageability
RIO	Rear Input/Output
RS-232	An Interface specified by Electronic Industries Alliance
RTC	Real Time Clock
RTM	Rear Transition Module
SBC	Single Board Computer
SDRAM	Synchronous DRAM
SFP	Small Form-factor Pluggable
SPD	Serial Presence Detect
SW	SoftWare
ULV	Ultra Low Voltage
XTM	Extension Module

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All product specifications are subject to change without notice.